MOTOROLA

HT 1000™, MT 2000™, MTS 2000™, and MTX Series

Handie-Talkie® Portable Radios

Theory / Troubleshooting Manual

CONTENTS

CONTENTS (cont.)

LIST OF TABLES

LIST OF FIGURES

RELATED PUBLICATIONS AVAILABLE SEPARATELY

Theory Manual (this publication) 68P81200C15

includes:

- theory of operation
- troubleshooting information and troubleshooting charts

Service Manual 68P81200C25

includes:

- all servicing information
- assembly / disassembly
- maintenance

Operating Instructions

- HT 1000 Portable Radios 68P81071C70
- MT 2000 Portable Radios 68P81076C65
- MTS 2000 I Portable Radios 68P81072C15
- MTS 2000 II and III Portable Radios 68P81072C45
- MTX Series Model B3 Privacy Plus Portable Radios 68P81072C10
- MTX Series Model B4 Privacy Plus Portable Radios 68P81073C60
- MTX Series Model B5 and B7 Privacy Plus Portable Radios 68P81072C40

Mobile Vehicular Adapter (MTVA) Operating Instructions 68P81075C85

Mobile Vehicular Adapter (MTVA) Installation Instructions 68P81075C90

Remote Speaker Microphones Operating Instructions 68P81073C40

GLOSSARY OF TERMS

ALC- Automatic Level Control; a circuit in the transmit RF path that controls RF power amplifier output, provides leveling over frequency and voltage, and protects against high VSWR

ASF IC- Audio Signalling Filter Integrated Circuit

Closed architecture- A controller configuration that utilizes a microcomputer with internal ROM, RAM, and EEPROM

DTMF- Dual Tone Multi-frequency

DPL- Digital Private-Line™

Firmware- Software or a software/hardware combination of computer programs and data, with a fixed logic configuration stored in a read-only memory; information can not be altered or reprogrammed

FGU- Frequency Generation Unit

FLASHport™- Is a Motorola term that describes the ability of a radio to change memory. Every FLASHport radio contains a FLASHport EEPROM memory chip that can be software written and rewritten to, again and again.

ISW- Inbound Signalling Word; data transmitted on the control channel from a subscriber unit to the central control unit

LSH- Low Speed Handshake; 150 baud digital data sent to the radio during trunked operation while receiving audio

MDC- Motorola Digital Communications

MRTI- Motorola Radio-Telephone Interconnect; a system that provides a repeater connection to the Public Switched Telephone Network (PSTN). The MRTI allows the radio to access the telephone network when the proper access code is received.

MSK- Minimum-Shift Keying

OMPAC- Over-Molded Pad-Array Carrier; a Motorola custom package, distinguished by the presence of solder balls on the bottom pads

Open architecture- A controller configuration that utilizes a microprocessor with extended ROM, RAM, and EEPROM

OSW- Outbound Signalling Word; data transmitted on the control channel from the central controller to the subscriber unit

PC Board- Printed Circuit Board

PL- Private-Line® tone squelch; a continuous sub-audible tone that is transmitted along with the carrier

PLL- Phase-Locked Loop; a circuit in which an oscillator is kept in phase with a reference, usually after passing through a frequency divider

PTT- Push-To-Talk; the switch located on the left side of the radio which, when pressed, causes the radio to transmit

Registers- Short-term data-storage circuits within the microcontroller

Repeater- Remote transmit/receive facility that re-transmits received signals in order to improve communications coverage

RESET- Reset line; an input to the microcontroller that restarts execution

RF PA- Radio Frequency Power Amplifier

RSSI- Received Signal Strength Indicator; a dc voltage proportional to the received RF signal strength

RPT/TA- Repeater/Talk-Around

RX DATA- Recovered digital data line

SCI IN- Serial Communication Interface Input line

SLIC- Support-Logic IC; a custom gate array used to provide I/O and memory expansion for the microprocessor

Softpot- Software potentiometer; a computer-adjustable electronic attenuator

Software- computer programs, procedures, rules, documentation, and data pertaining to the operation of a system

SPI (clock and data lines)- Serial Peripheral Interface; how the microcontroller communicates to modules and ICs through the CLOCK and DATA lines

Squelch- Muting of audio circuits when received signal levels fall below a pre-determined value

SRAM- Static-RAM chip used for scratch-pad memory

Standby mode- An operating mode whereby the radio is muted but still continues to receive data

System central controller- Main control unit of the trunked dispatch system; handles ISW and OSW messages to and from subscriber units (see ISW and OSW)

System select- The act of selecting the desired operating system with the system-select switch (also, the name given to this switch)

TOT- Time-Out Timer; a timer that limits the length of a transmission

TSOP- Thin Small-Outline Package

µC- Microcomputer

µP- Microprocessor

VCO- Voltage-Controlled Oscillator; an oscillator whereby the frequency of oscillation can be varied by changing a control voltage

VCOB IC- Voltage-Controlled Oscillator Buffer Integrated Circuit

VSWR- Voltage Standing Wave Ratio

INTRODUCTION

I. PURPOSE

This manual will provide a theoretical explanation of the HT 1000, MT 2000, MTS 2000, and MTX Series portable radio's operation, troubleshooting, and additional useful information about the radio not found in any other publication. The manual is divided into three sections:

- INTRODUCTION
- THEORY OF OPERATION
- TROUBLESHOOTING

In the THEORY OF OPERATION section, a basic functional description is followed with a more detailed description of some selected circuits. All applicable frequency bands are covered in this publication.

A complete list of models and each model's description is provided in a separate service manual. A detailed description of the radio's operational features, a list of applicable batteries and accessories, and a section on general radio information is provided in several operating instruction manuals. To help you with your selection, a complete list of the other publications on HT 1000, MT 2000, MTS 2000, and MTX Series portable radios can be found following the Table of Contents of this manual.

II. DESCRIPTION

A. General

The HT 1000 Handie-Talkie portable radio is a microcomputer-based, single-mode (conventional) transceiver. The MT 2000, MTS 2000, and MTX Series Handie-Talkie portable radios are microprocessor-based dual-mode (trunked/conventional) transceivers. In all of the radios, the microcomputer determines the active state of the radio (transmit/receive), monitors radio status, and processes operator commands entered from the keypad (if applicable) or the other radio controls.

Various switches, buttons, knobs, and indicators are ergonomically designed, making placement in strategic locations on the different model radios. Refer to the specific operating instructions on your radio for location and description of these controls. All of the controls, including the push-to-talk (PTT) switch and key pad (if applicable) are weather resistant. The microphone and speaker are covered by a diaphragm for additional protection.

B. Printed Circuit Boards and Flexible Circuits

Most of the radio circuitry is contained in chip carriers that are mounted on one of the two rigid, printed circuit boards (PC boards); the controller board and the transceiver board. Front display model radios contain a third rigid PC Board; the keypad/display board, which is a two-sided board supporting the DTMF keypad, and a 14-character, dot-matrix display. This board is not field serviceable. If a fault develops with the keypad, display, or backlights, the entire board must be replaced. Also, the top-display model radios contain a small display board located under the top escutcheon. This provides 2-character, 6-segment, starburst-type display. This board is not field serviceable. The entire board must be replaced.

All discrete wiring has been replaced with flexible circuits: a controls flex, a front cover/display flex, and a jumper flex. The controls flex interconnects the top controls and the side controls (PTT switch, emergency push button, telephone-interconnect push button) with the controller board. The front cover/display flex routes signals between the controller, the 13-pin universal connector, the front cover components (speaker and microphone), and if applicable, the display/keypad board. The jumper flex routes signals between the transceiver and the controller board.

THEORY OF OPERATION (BASIC FUNCTIONAL DESCRIPTION)

I. INTRODUCTION

This publication covers a large family of portable radios: HT 1000, MT 2000, MTS 2000, and MTX series units. They are software driven, and because of the wide range of operating systems and radio functionality provided by this family of radios, the theory discussions will be divided into several major categories. The transceiver is frequency sensitive and falls into one of four frequency bands: vhf, uhf, 800MHz, or 900MHz. Because of their similarity, transceivers will be categorized into two discussion groups: vhf/uhf transceivers and 800/900MHz transceivers. The controller falls into two categories: a closed architecture controller and an open architecture controller. Each controller will be discussed separately. This THEORY OF OPERATION section of the manual provides a functional description of the radio. First, overall radio functions are discussed in basic terms, with each circuit and its relationship to other parts of the radio described. Then, a more detailed functional description is given for circuit relationships, with special attention directed to some of the selected circuits. Pay particular attention to the topics being discussed, and note the application: **vhf/uhf** transceiver, **open** architecture controller, etc.

II. RADIO POWER

A. General

In this family of radios, power is distributed to four general combinations of transmitters and controllers:

1. vhf/uhf xcvr with closed architecture controller
2. vhf/uhf xcvr with open architecture controller
3. 800/900MHz xcvr with closed architecture controller
4. 800/900MHz xcvr with open architecture controller

Discussing each of the four combinations would be somewhat redundant, so pairs 1 and 4 were chosen for illustration and explanation in the following paragraphs. Paragraph B covers the vhf/uhf transceiver and the closed architecture controller; paragraph C covers the 800/900MHz transceiver and the open architecture controller.

B. B+ Routing and DC Voltage Distribution (for a Closed Architecture Controller and a VHF or UHF Transceiver)

Operating power for the radio is derived from a 7.5-volt battery (BATT 7.5V), which is applied directly to the transceiver board as B+. The B+ voltage is fused and routed through the jumper flex as Raw B+ and applied through the controller board to the controls flex. In the controls flex, B+ is applied to the on/off/volume control. When the radio is turned on, switched B+ (SB+) and the voltage sources required to operate various stages of the radio are distributed as shown in Figure1A.

The power amplifier (PA) module (U105) and automatic level control (ALC) IC (U101) of the RF board are powered-up directly from the BATT B+. Other sections of the transceiver board are powered-up through the switched B+. Two 5-volt regulators are used on the transceiver board; one 5V regulator (U202) is used to supply those circuits which require voltages to be on all the time, such as the reference oscillator, synthesizer IC, IF IC, and digital-to-analog (D/A) IC. The voltage-control oscillator (VCO) buffer obtains its voltage (Vcc) from the SOUT line of the synthesizer. The other 5V regulator (U103) of the transceiver board supplies 5V to the receiver RF AMP IC and Mixer IC during the receive mode and to the ALC and other transmitter circuitry during the transmit mode.

The controller board obtains its voltage source from switched B+, and produces regulated 5 volts from two regulators. One 5V regulator (U709) is used to supply 5V to the microcomputer. The SB+ is also connected to the AUDIO PA. The audio signalling filter (ASF) IC obtains its 5V (Vcc) from the AUDIO PA (U706) internal 5V regulator.

C. B+ Routing and DC Voltage Distribution (for an Open Architecture Controller and an 800 or 900MHz Transceiver)

Refer to figure 1B and note that operating power for the radio is derived from a 7.5-volt battery (BATT 7.5V), which is applied directly to the transceiver board as B+. The B+ voltage is fused and routed through the jumper flex as Raw B+ and applied to the controller board. From the controller, B+ is applied to three different areas:

1. the expansion board, via connector jack J702 pin1,
2. an electrical switch IC, U712 pins 2 and 3, and
3. the controls flex, via connector jack J703 pin 8.

The UNSW B+ is routed to the expansion board so that functions there can be performed independently of the SW B+ supply. The UNSW B+ is also routed to the electrical switch IC, U712 (a P-channel FET in an SOIC-8 package), which connects it to SW B+ when the control voltage at U712 pin 4 is low. The SW B+ is then distributed to the rest of the radio, including the transceiver board, front cover/display flex, and expansion board, as well as other controller board circuitry. Finally, UNSW B+ is routed to the mechanical on/off switch and returns to the controller as MECH SWB+. The MECH SWB+ signal activates the electrical switch (U712), and also feeds a resistive divider so that the microprocessor (U705) can monitor the battery voltage.

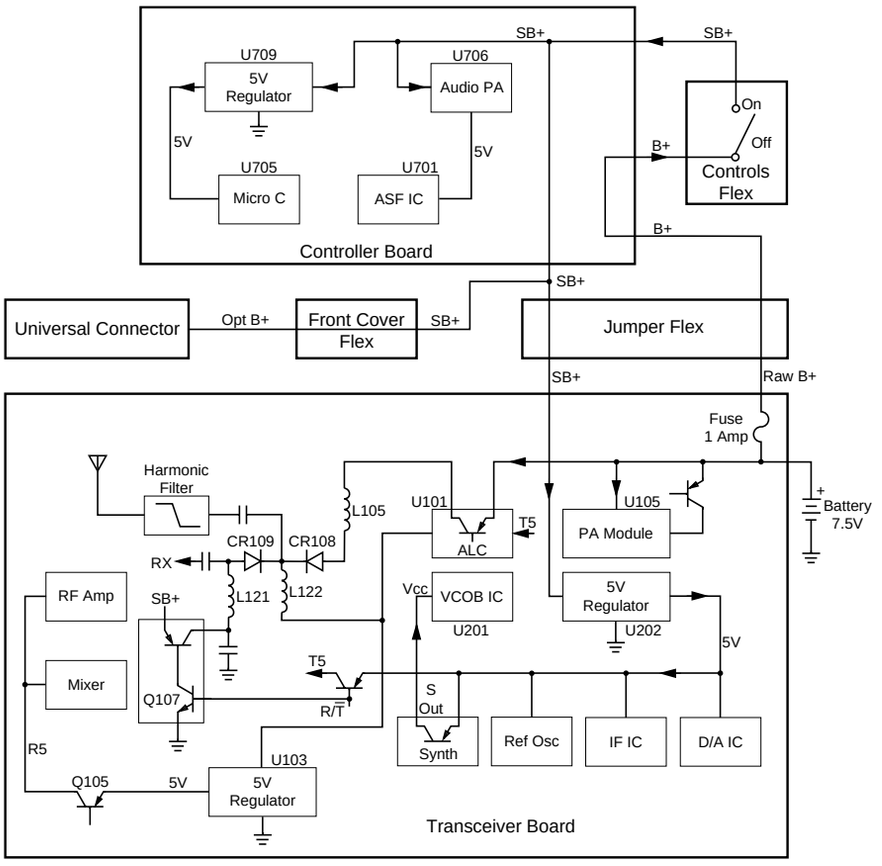


Figure 1A. DC Power Distribution Block Diagram (Closed Architecture Controller and VHF or UHF Transceiver)

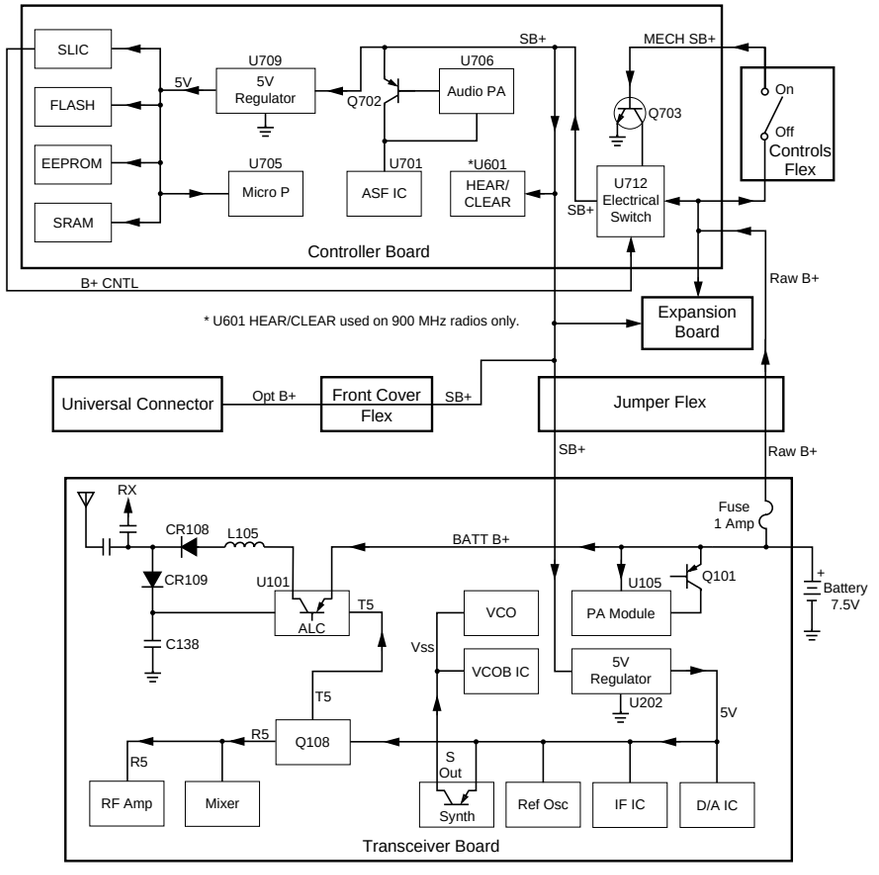


Figure 1B. DC Power Distribution Block Diagram (Open Architecture Controller and 800 or 900MHz Transceiver)

In the transceiver, SWB+ is routed directly to the 5v regulator (U202). The regulated 5v supplies the IF IC (U3), the reference oscillator (U203), the Fractional-N synthesizer IC (U204), the D/A IC (U102), and the R/T switch (Q108).

Internal to the synthesizer is a superfilter which supplies the VCO module (U205) and the VCO buffer IC (U201) with 4.6 volts, produced by the regulated 5V supply.

In addition, two more 5-volt supplies exist, one for transmit and one for receive: T5 and R5, respectively. The regulated 5v is switched to either one or the other by transistor Q108, under the control of the D/A IC. The T5 voltage is used as a control line by the TX ALC IC and provides bias for the RF PA input and the external antenna connector. The R5 voltage is supplied to the RF amplifier (U1) and the Mixer Buffer IC (U2).

III. VHF/UHF TRANSCEIVER BOARD

A. Frequency Generation Unit (See Figure 2)

The frequency generation unit (FGU) consists of three major sections: the high stability reference oscillator(U203), fractional-N synthesizer (U204), and VCO buffer IC(U201). The VCO provides the carrier frequency for the transmitter (TX OUT), and provides the local oscillator (LO) injection signal for the receiver mixer buffer (RX OUT).

The RX VCO uses an external active device, whereas the TX VCO uses the internal device of the VCO buffer IC. The phase lock loop (PLL) circuit is provided by the fractional-N synthesizer IC.

The output of the VCO is amplified by the prescaler buffer, routed through a low-pass filter, and applied to the prescaler divider of the synthesizer. The divide ratios are determined from information stored in memory that was bussed to the synthesizer via the microcomputer. The microcomputer extracts data for the division ratio as determined by the channel select switch. The resultant VCO buffer signal is applied to a comparator in the synthesizer. The synthesizer comparator also receives a reference frequency via a reference divider input from the 16.8 MHz temperature-compensated reference oscillator. If the two frequencies differ, the synthesizer generates a control (error) voltage which causes the VCO to change frequency.

Modulation of the carrier is achieved by using a 2-port modulation technique. The deviation of the low frequency tone, such as DPL/TPL, is achieved by injecting the signal to an analog/digital circuit in the synthesizer. The resultant digitized signal is then modulated by the fractional N-divider, thus generating the required deviation. The deviation of the high frequency tone is achieved by modulating the modulation varactor on the VCO. In order to cover a very wide bandwidth, the VCO control voltage is stepped up by using a positive and negative multiplier circuit. A 13-volt supply powers the phase detector circuitry. The VCO signal is amplified by the integrated buffer amplifier of the VCO buffer. The two output signals, receiver first LO injection and transmitter carrier frequency, are filtered and then routed to the mixer/buffer (U2) and the RF PA (U105), respectively.

B. Antenna Switch

The function of the antenna switch is to route the transmitter power to the antenna during the transmit mode, or route RF from the antenna to the receiver front end during the receive mode.

C. Receiver Front End (See Figure 3)

The RF signal from the antenna is coupled to the first bandpass filter through the antenna switch. The output of the bandpass filter is then applied to a wideband RF amplifier IC (RF AMP). The bandpass filter is electronically tuned by the D/A IC, which is controlled by the microcomputer. Wideband operation of the filter is achieved by retuning the bandpass filter across the band. After amplification, the RF signal is further filtered by a second fixed-tuned filter to improve the spurious rejection.

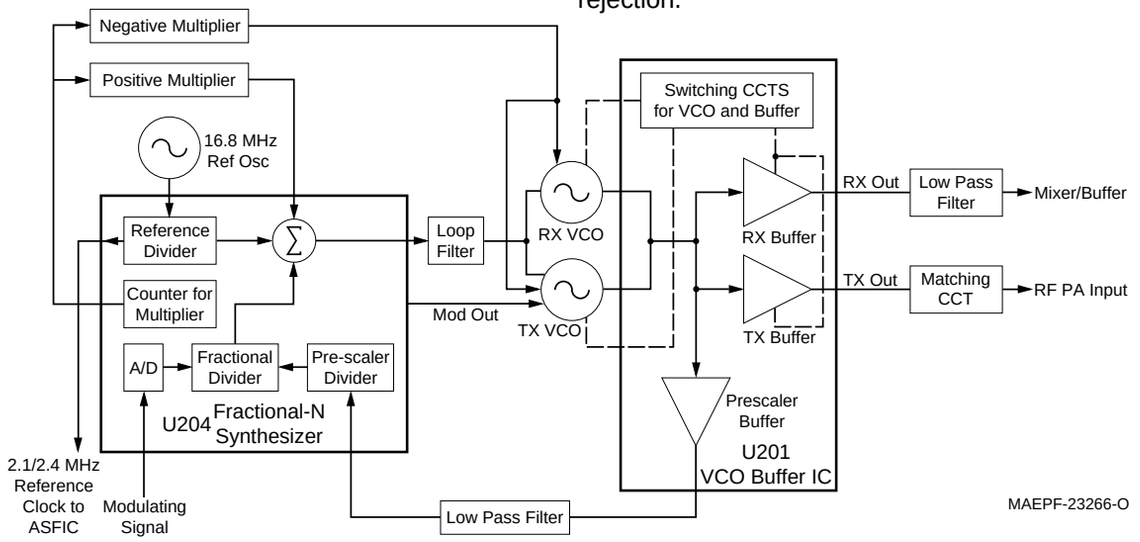


Figure 2. VHF/UHF Frequency Generation Unit (FGU) Circuits

The filtered RF signal is then applied to the RF input of a broadband mixer IC. An injection signal (FIRST LO), supplied by the FGU, is applied to the second input of the mixer stage. The resulting difference frequency (44.85MHz for VHF and 73.35MHz for UHF), is the first IF frequency. The first IF frequency is then filtered by a 2-pole crystal filter to remove unwanted mixer products and routed to the IF IC.

D. Receiver Back End (See Figure 3)

In the IF IC, the first IF frequency is down converted, amplified, filtered, and demodulated to produce the recovered audio. The IF IC is electronically programmable, and the amount of filtering, which is dependent on the radio channel spacing, is controlled by the microcomputer. Additional filtering, which used to be provided externally by a conventional ceramic filter, is replaced by internal filters in the IF IC. The IF IC uses a type of direct conversion process where the second LO frequency is very close to the first IF frequency. The IF IC controls the second LO VCO and causes the VCO to track the first IF frequency, producing a phase-locked operation. The IF IC also provides a recovered signal-strength indicator (RSSI) and squelch output for use in other parts of the radio.

E. Transmitter (See Figure 4)

The transmitter consists of the following stages:

- Harmonic Filter
- RF Power Amplifier
- ALC IC, which controls the power output

Harmonics of the carrier frequency are generated by the PA module and antenna switch. The harmonic filter circuit attenuates the unwanted signals.

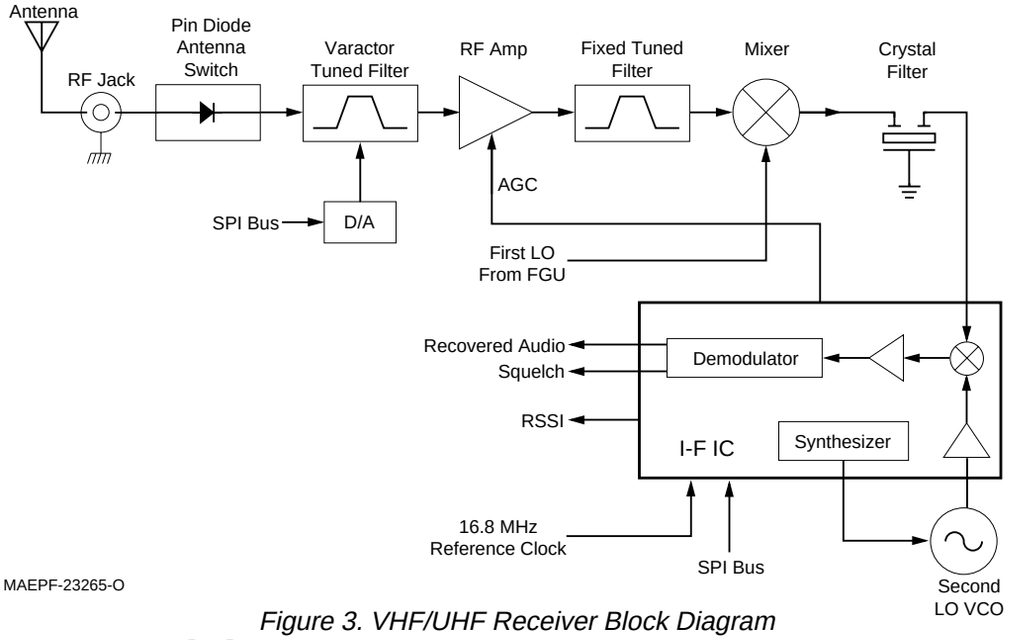


Figure 3. VHF/UHF Receiver Block Diagram

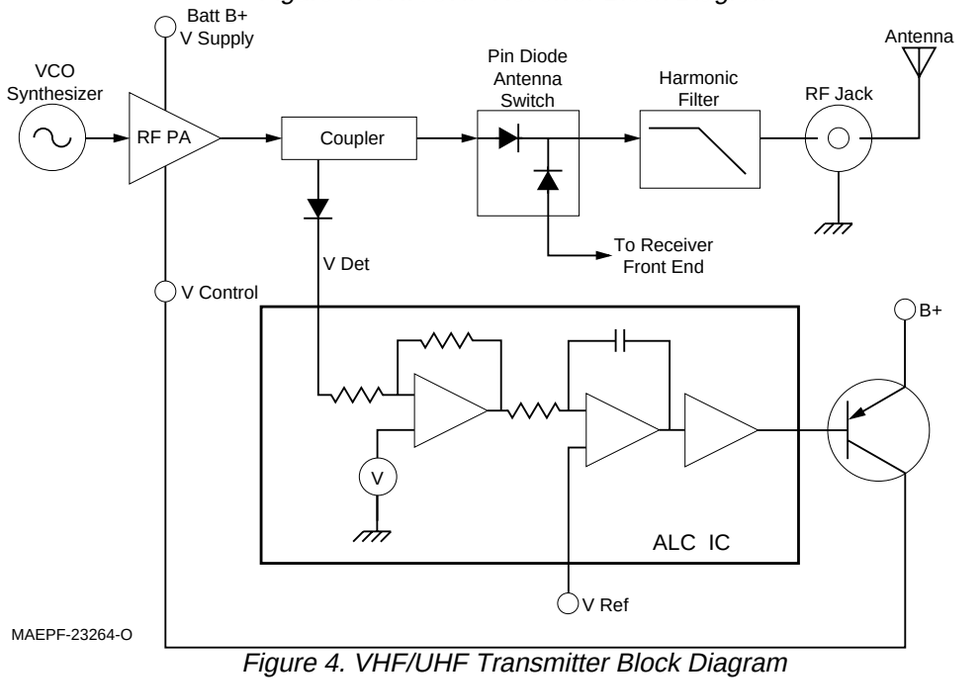


Figure 4. VHF/UHF Transmitter Block Diagram

The RF PA module is a multi-stage amplifier, which has the required gain to produce an output level of several watts. Some harmonic filtering is accomplished in the RF PA.

Power control is achieved by using the coupler detector to feed back a portion of the PA output to the ALC circuit. This ALC circuit increases or decreases the overall PA gain as appropriate. Another function of the detector is to provide a signal when the VSWR exceeds the threshold level. This signal, combined with the forward detected power, is used to reduce the PA output power, thus protecting the PA under high VSWR conditions.

IV. 800/900MHz TRANSCEIVER BOARD

A. Frequency Generation Unit (See Figure 5)

The frequency generation unit (FGU) consists of the following major sections: the high stability reference oscillator (U203), fractional-N synthesizer (U204), VCO buffer IC (U201), and VCO (U205). The VCO provides the carrier frequency for the transmitter (TX OUT), and provides the local oscillator (LO) injection signal for the receiver mixer buffer (RX OUT). The phase lock loop (PLL) circuit is provided by the fractional-N synthesizer IC.

The output of the VCO is amplified by the prescaler buffer, routed through a low-pass filter, and applied to the prescaler dividers of the synthesizer. The divide ratios are determined from information stored in memory that is bussed to the synthesizer via the microprocessor. The microprocessor extracts data for the division ratio as determined by the channel-select switch. The resultant VCO buffer signal is applied to a comparator in the synthesizer. The synthesizer comparator also receives a reference frequency via a reference divider input from the 16.8 MHz temperature-compensated reference oscillator. If the two frequencies differ, the synthesizer generates a control (error) voltage which causes the VCO to change frequency.

Modulation of the carrier is achieved by using a 2-port modulation technique. The deviation of the low frequency tone, such as DPL/TPL, is achieved by injecting the signal to an analog/digital circuit in the synthesizer. The resultant digitized signal is then modulated by the fractional N-divider, thus generating the required deviation. The deviation of the high frequency tone is achieved by modulating the modulation varactor on the VCO. In order to cover a very wide bandwidth, the VCO control voltage is stepped up by using a positive multiplier circuit. A 13-volt supply powers the phase detector circuitry. The VCO signal is amplified by the integrated buffer amplifier of the VCO buffer. The two output signals, receiver first LO injection and transmitter carrier frequency, are filtered and then routed to the mixer/buffer (U2) and the RF PA (U105), respectively.

B. Antenna Switch

The function of the antenna switch is to route the transmitter power to the antenna during the transmit mode, or route the RF from the antenna, to the receiver front end during the receive mode.

C. Receiver Front End (See Figure 6)

The RF signal from the antenna is coupled to the first bandpass filter through the antenna switch. The output of the bandpass filter is then applied to a wideband RF amplifier IC (RF AMP). The bandpass filter is a wideband stripline filter, which is pretuned for the frequency band. After amplification, the RF signal is further filtered by a second fixed-tuned stripline filter to improve the spurious rejection.

The filtered RF signal is then applied to the RF input of a broadband mixer IC, U2. An injection signal (FIRST LO) supplied by the FGU, is applied to the second input of the mixer stage. The resulting difference frequency of 73.35MHz is the first IF frequency. The first IF frequency is then filtered by a 2-pole crystal filter, FL1, to remove unwanted mixer products and routed to the IF IC, U3

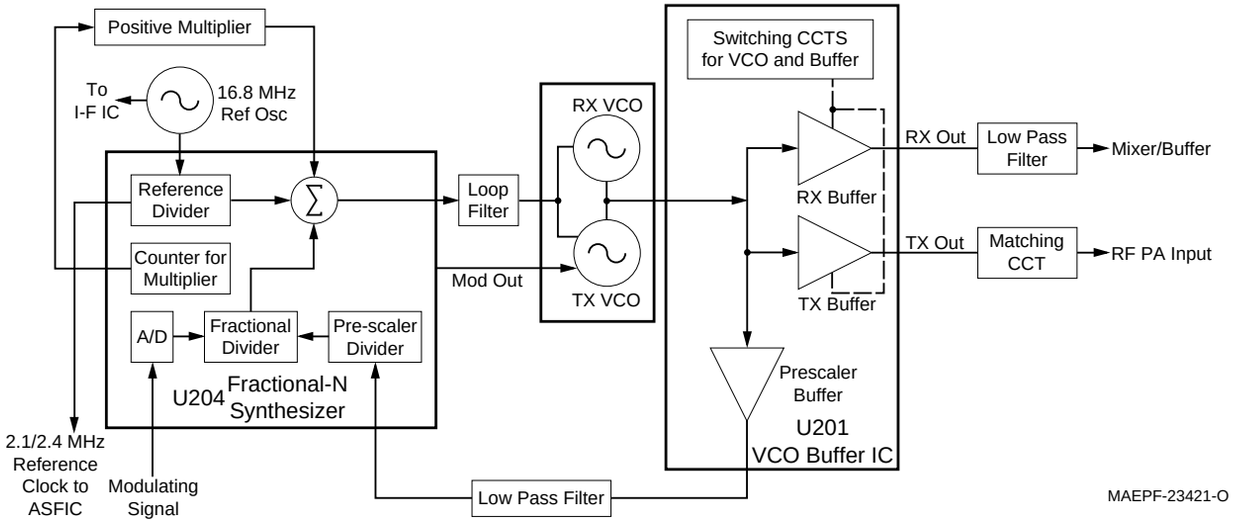


Figure 5. 800/900MHz Frequency Generation Unit (FGU) Circuits

D. Receiver Back End (See Figure 6)

In the IF IC, the first IF frequency is down converted, amplified, filtered, and demodulated to produce the recovered audio. The IF IC is electronically programmable, and the amount of filtering, which is dependent on the radio channel spacing, is controlled by the microprocessor. Filtering is accomplished by internal filters in the IF IC. The IF IC uses a type of direct conversion process where the second LO frequency is very close to the first IF frequency. The IF IC controls the second LO VCO and causes the VCO to track the first IF frequency, producing a phase-locked operation. The IF IC also provides a recovered signal-strength indicator (RSSI) and squelch output for use in other parts of the radio.

E. Transmitter (See Figure 7)

The transmitter consists of the following stages:

- Low-pass antenna matching circuit
- RF Power Amplifier
- ALC IC and coupler, for power output control

The low-pass antenna matching circuit attenuates RF PA harmonics, and provides the optimum phase load to the RF PA. The RF PA module is a multi-stage amplifier, which has the required gain to produce an output level of several watts. Some harmonic filtering is also accomplished in the RF PA.

Power control is achieved by using the coupler detector to feed back a portion of the PA output to the ALC circuit. This ALC circuit increases or decreases the

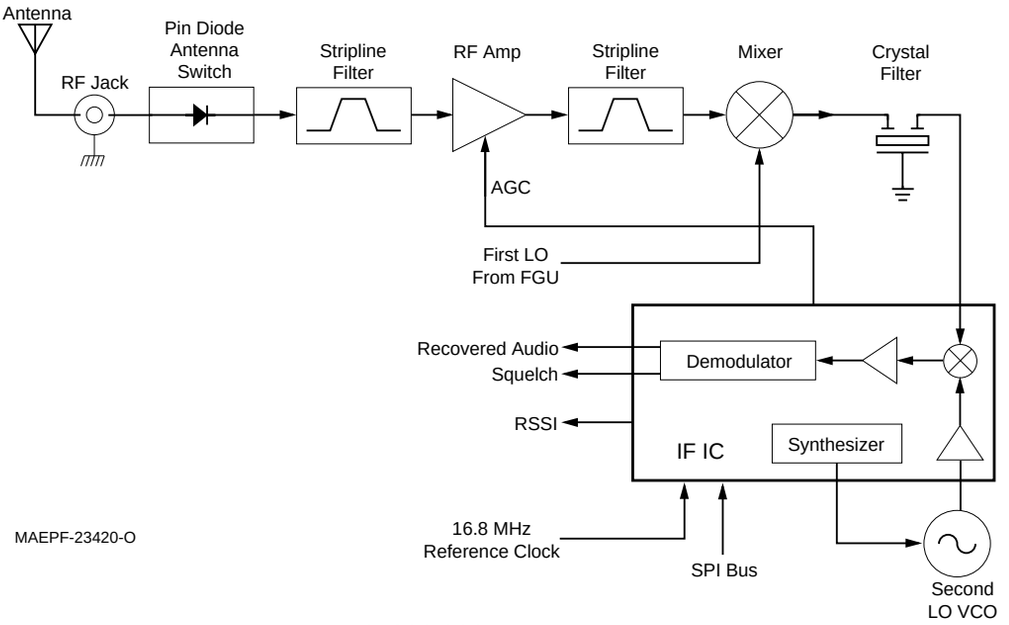


Figure 6. 800/900MHz Receiver Block Diagram

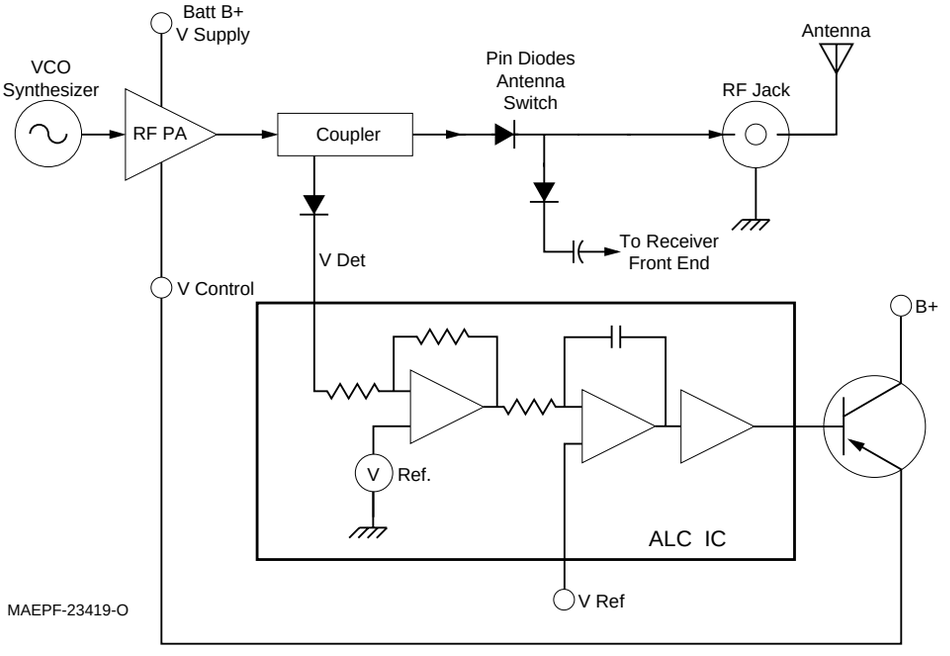


Figure 7. 800/900MHz Transmitter Block Diagram

overall PA gain as appropriate. Another function of the detector is to provide a signal when the VSWR exceeds the threshold level. This signal, combined with the forward detected power, is used to reduce the PA output power, thus protecting the PA under high VSWR conditions.

V. CLOSED ARCHITECTURE CONTROLLER

A. General (See Figure 8)

The controller board is the central interface between various subsystems of the radio. It is segregated into digital and audio architecture. The digital portion consists of a special Motorola microcomputer. The audio power amplifier (AUDIO PA) and audio/signalling/filter IC (ASF IC) form the backbone of the audio/signalling architecture. The controller board has its own voltage regulators to generate 5 volts, sourced by switched B+ from the battery.

B. Digital Architecture

The Motorola microcomputer consists of 640 bytes of EEPROM, 760 bytes of RAM, and 24k of ROM. The microcomputer executes the radio software and monitors the activity of all user interfaces. Using the communication buses, the microcomputer handles the responsibility of programming all applicable ICs in the radio, including those on the RF transceiver board. This programming sets up the ICs to properly perform a variety of functions, such as what frequency to transmit or what channels to scan. The digital circuitry is powered by a discrete 5-volt regulator to help isolate the digital signals from the audio signals in nearby circuits.

C. Audio Signalling Architecture

A Motorola custom IC (ASF) provides both transmit and receive audio and signalling processing. The ASF IC is programmable by the microcomputer via the serial peripheral interface (SPI). It provides filtering on both transmit and receive audio, and also provides PL, DPL, and MDC encoding and decoding.

In the transmit mode, the ASF IC amplifies, shapes, limits, and filters the outgoing signal. The processed signal is sent to the transceiver board's FGU. In the receive mode, the demodulated signal from the receiver back end is amplified, filtered and routed to the AUDIO PA for amplification. The ASF IC provides pre-emphasis and de-emphasis as well as squelch. Based on a reference signal from the transceiver board, the ASF IC provides the microcomputer with a clock signal.

Received audio signal amplification is achieved by the AUDIO PA IC. The IC's output drives the radio's internal speaker, or an external speaker connected via an option cable. In order to minimize the effects, and to further isolate the audio signals from the digital signals, the audio section has its own isolated 5V regulator on the AUDIO PA.

VI. OPEN ARCHITECTURE CONTROLLER

A. General (See Figure 9)

The controller board is the central interface between various subsystems of the radio. The controller board is composed of both digital and audio circuits. The digital portion consists of a special Motorola microprocessor (U705), a custom, gate-array, memory-support-logic IC (SLIC), U710, and the memory devices (U713, U714, and U715). The audio circuits include the audio power amplifier (U702), the audio/signalling/filter IC (ASF IC), U701, and in the 900MHz radios, the Hear Clear IC, U601. The controller board has its own voltage regulators to generate 5 volts, sourced by switched B+ from the battery. The open architecture controller board also has a plug-in interface for secure voice encryption options, and another interface for the display and keypad version radios.

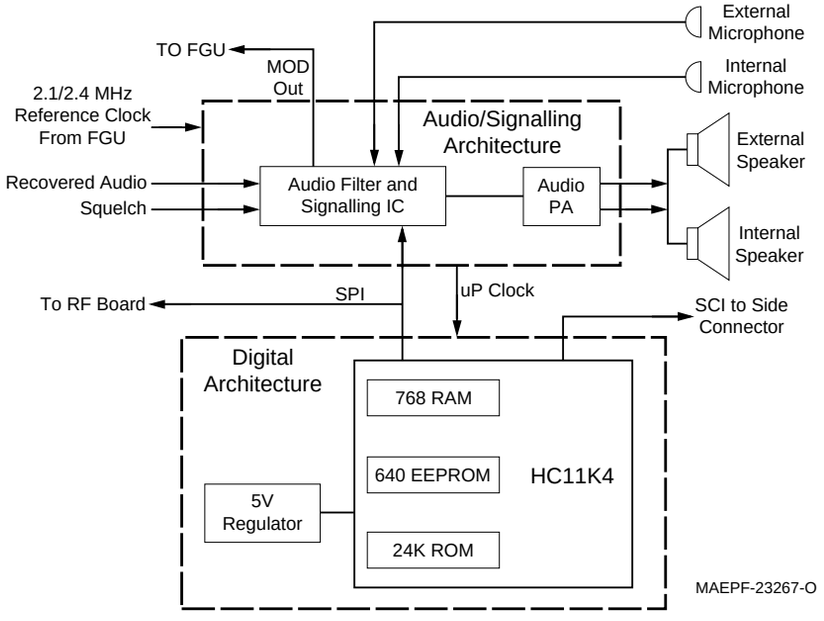
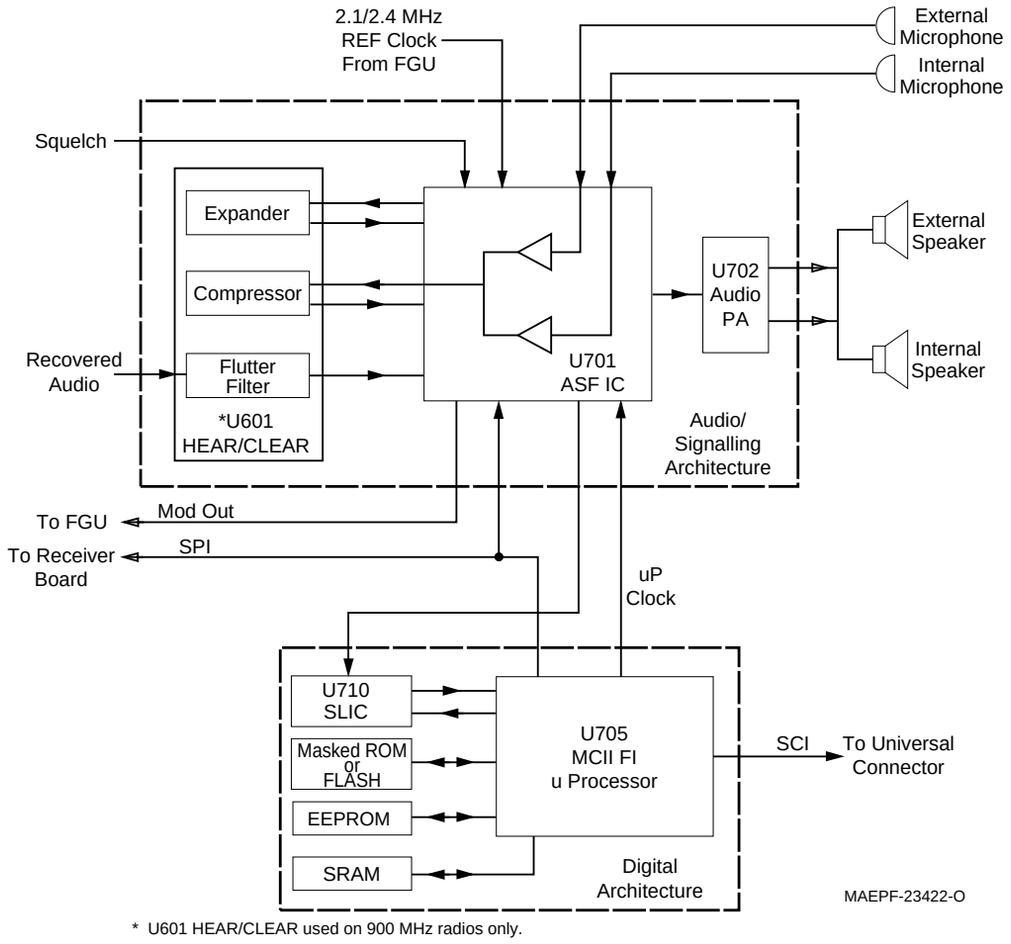


Figure 8. Closed Architecture Controller Block Diagram



* U601 HEAR/CLEAR used on 900 MHz radios only.

Figure 9. Open Architecture Controller Block Diagram

B. Digital Architecture

The Motorola microprocessor, in conjunction with the SLIC, performs the functions of controlling the internal workings of the radio, as well as interfacing with the outside world. The microprocessor has 1K of RAM and 512 bytes of EEPROM on the chip. In some versions the controller board enhances the capabilities of the microprocessor chip by providing 256K or 512K of FLASH memory, 32K static RAM, and 8K or 32K of EEPROM. Other versions use masked programmed ROM.

The “FLASH” open controller is flexible and capable of firmware being reprogrammed to support future features. The controller, through communication busses, programs all applicable ICs in the radio (including those on the transceiver board) for proper operation in the designated frequency band.

C. Audio Signalling Architecture

The Motorola custom integrated circuit, ASF IC, performs audio signal shaping and filtering. The ASF IC also encodes and decodes Private-Line (PL), Digital Private-Line (DPL), and Motorola Digital Communication (MDC) signals, as well as decoding trunking signals.

In the transmit mode, the ASF IC amplifies and shapes the modulating signal on its way to the modulating port of the FGU. In the receive mode, the ASF IC amplifies and filters the demodulated signal and applies it to the audio PA, which drives the internal or external radio speaker. The ASF IC not only performs pre-emphasis and de-emphasis, but also performs the squelch functions and provides the microprocessor with a clock signal.

THEORY OF OPERATION (DETAILED FUNCTIONAL DESCRIPTION)

I. INTRODUCTION

In this section of the of the manual, a more detailed description of the radio and some special circuit is given. For a better understanding of the circuits descriptions, and to aid in following the text, refer to the applicable schematic diagram(s) in the corresponding service manual (Motorola part number 68P81200C25), or previously 68P81200C20.

II. RADIO POWER

A. General

As previously described in the THEORY OF OPERATION (BASIC FUNCTIONAL DESCRIPTION) RADIO POWER paragraph, power is distributed to four general combinations of transmitters and controllers:

1. VHF/UHF transceiver with closed architecture controller,
2. VHF/UHF transceiver with open architecture controller,
3. 800/900MHz transceiver with closed architecture controller, and
4. 800/900MHz transceiver with open architecture controller

Discussing each of the four combinations would be somewhat redundant, so pairs 1 and 4 were chosen for explanation in the following paragraphs. Paragraph B covers the vhf/uhf transceiver and the closed architecture controller; paragraph C covers the 800/900MHz transceiver and the open architecture controller.

B. B+ Routing and DC Voltage Distribution (for a Closed Architecture Controller and a VHF or UHF Transceiver)

Raw B+ (7.5V) from the battery (Batt B+) enters the radio on the transceiver board through a 3-contact spring pin arrangement (P404) as B+, where it is routed directly to the RF PA Module and ALC IC pin 13. Battery B+ is fused, and then routed through the jumper flex (P704, pins1 and 20) to the controller board (J704, pins 1 and 20). The B+ supply is routed through the controller board to the on/off/volume control (S403/ R401) on the controls flex at jack J703, pin 8. With the mechanical on/off switch (S403) placed in the on position, switched B+ (SB+) is routed from the controls flex at connector plug P703, pin 10 and applied to the controller at connector jack J703, pin10. This signal is also fed to a resistive divider R708, R709 so that the microcomputer (U705) can monitor the battery voltage.

The SB+ voltage powers the audio PA (U706) and its internal 5V regulator booster transistor (Q702). It also powers a discrete 5V regulator (U709). Regulated 5 volts from module U709 powers the microcomputer (U705) and other digital circuitry. The ASF IC (U701) obtains its 5V (Vcc) from the AUDIO PA internal 5V regulator through a booster transistor (Q702)

The switched B+ voltage supplies power to circuits on the transceiver board. The 5-volt regulator, U202, is applied this voltage through decoupling component C125 to produce a stable 5.0 volt output. Raw B+ (7.5V) which is connected to the ALC IC (U101), is switched through the output (CATH1) to another 5-volt regulator (U103).

Regulator U202 supplies those circuits which need to remain on at all times, such as the reference oscillator (U203), fractional-N-synthesizer (U204), D/A IC (U102), and the IF module (U3). The D/A IC controls dc switching of the transceiver board. The SC1 signal at U102 pin 12 controls transistors Q107, Q104, and the transmit 5 volts (T5). The SC3 signal at U102 pin 14 controls transistor Q105, and the receive 5 volts (R5). A voltage on the synthesizer SOUT line at U204 pin 19 supplies power (Vcc) to the VCO buffer at U201 pin 3.

During the receive mode, via switching transistor Q105, regulator U103 supplies regulated 5V (R5) to the receiver front end. In the battery-saver mode, R5 can be switched on and off by controlling pin 1 of transistor Q105. Module U103 is not used during the transmit mode. During the transmit mode, transmit 5 volts (T5) for the ALC IC and other TX circuitry is obtained from U202 via switching transistor Q104.

1. Low-Battery Detect Circuit (Controller Board)

   The low-battery detect circuit generates an audio alert when the radio's battery needs recharging. The implementation of this function takes advantage of the microcomputer's on-chip, 8-bit, 8-channel, A/D converter, U705 pins PE0-PE7. The 7.5V (SB+) is divided down to a nominal 3.92V by resistors R708 and R709, and fed to port PE4 of U705. This voltage is converted by the A/D converter to a digital format. The microcomputer compares this voltage to a preset low-battery trip threshold, which corresponds to a battery voltage of ≅7.0V in standby or ≅6.2V in transmit. If the measured voltage is lower than either threshold, the low battery alert tone is generated (if option is enabled) to warn the user that approximately 20 minutes of usable battery capacity remains.

2. Power for External Accessories

   Via current limiting resistor R733 and associated isolation and protection components VR715, VR720, and C709, SB+ is available on the controller board at connector jack J701 pin 16. From the controller board, SB+ is routed through the front-cover flex (P701 pin 16 to J403 pin 4) and applied to to the universal connector at P403 pin 4 as OPT B+.

The OPT B+ voltage powers external accessories used with the radio.

C. B+ Routing and DC Voltage Distribution (for an Open Architecture Controller and an 800 or 900MHz Transceiver)

This radio differs from previous Motorola portable radios in that B+ from the battery is electrically switched to most of the radio, rather than routed through the on/off/volume switch, S403/R401. The electrical switching of B+ supports a "keep-alive" mode. Under software control, even when the on/off switch has been turned to the off position, power remains on.

Raw B+ (7.5V) from the battery (Batt B+) enters the radio on the transceiver board through a 3-contact spring pin arrangement (P404) as B+, where it is routed through two ferrite beads (E102 and E101) and applied to the RF PA and the ALC IC on pin 13. Battery B+ is fused, and is then routed to the controller board, where it enters on connecter J704 pins 1 and 20. From the controller, BATT B+ fans out to three different areas: (1) the secure or data option board via connector jack J702 pin 1, (2) the electrical switch IC, U712 pins 2 and 3, and (3) the control-top flex via connector jack J703 pin 8. UNSW B+ is routed to the secure board so that it can perform key management and other functions independently of SW B+. UNSW B+ is routed to the electrical switch IC, U712 (a P-channel FET in an SOIC-8 package), which connects it to SW B+ when the control voltage at U712 pin 4 is low. SW B+ is then distributed to the rest of the radio, including the transceiver board, the display/keypad board, and the secure or data option board, as well as other controller board circuitry. Finally, UNSW B+ is routed to the mechanical ON/OFF switch via connector jack J703 pin 8, and returns to the controller as MECH SWB+ (J703 pin 10). This signal is used to activate the electrical switch (U712), and also is fed to a resistive divider so that the microprocessor (U705) can monitor the battery voltage.

The electrical switch (U712) is activated by transistor Q703, which in turn is driven by either the MECH SWB+ or the B+ CNTL signals turning on one or both of the diodes in CR704. Let us consider what happens when the radio is initially off and all circuits are powered down. When the user switches the ON/OFF switch to the ON position, the MECH SWB+ signal will be connected to UNSW B+ and transistor Q702 will then be turned on. Transistor Q703 pin 3 will go low (< .3 V), and this will turn on U712, which in turn connects UNSW B+ to SW B+. The SW B+ will then be fed to all the other radio circuitry, and the radio will begin its normal power-on sequence. In particular, the microprocessor, U705, will initialize after regulated Vdd from U708 reaches 5.0 V. It can then program the gate array (U710) so that the B+ CNTL signal can be an output high or low (initially this pin, U710-G8, is configured as an input so that it does not drive diode CR704).

Recalling that SW B+ to the radio is controlled by U712, which is activated by the B+ CNTL signal or MECH SWB+ via CR704 and Q702, if the user turns off the ON/OFF switch then MECH SWB+ drops to zero volts. If the microprocessor has set B+ CNTL to logic zero, then Q702's inverted output (pin 3) will be high, and the power switch (U712) will turn off, and SW B+ will drop to zero. If, however, the controller is programmed to support power-down de-affiliation (typically for a trunked system only), then it will have left B+ CNTL at a logic high. In this case, when the ON/OFF switch is turned off, SW B+ will continue to be supplied to the radio, but the microprocessor will sense that the switch has turned off by reading that the voltage on pin U705-PE1 has fallen to zero. The microprocessor can then key up the transmitter and send a de-affiliation ISW to the trunking system. After receiving and verifying an acknowledgement, the microprocessor then shuts down SW B+ (and therefore, its own power, since Vdd comes from SW B+ via U708) by setting B+ CNTL=0. In summary, we see that turning the ON/OFF switch ON always supplies power to the radio circuitry, but the radio can only power down when the switch is OFF and the microprocessor has set B+ CNTL=0.

1. Low-Battery/ Detect Circuit (Controller Board)

   The low-battery detect circuit is used to warn the user that the radio's battery needs recharging. The implementation of this function on open architecture radios takes advantage of the microprocessor's on-chip 8-bit, 8-channel A/D converter (pins PE0-PE7 of U705). The mechanically switched 7.5V (MECH SWB+) is divided down to a nominal 3.92 V by resistors R725 and R726 and fed to port PE1 of U705. This voltage is converted by the A/D to digital format. The microprocessor compares this voltage to a preset low-battery trip threshold, which corresponds to a battery voltage of ≅7.0V in standby mode or ≅6.20V in transmit mode. If the measured digitized voltage is lower than either low battery threshold, the low battery alert tone or flashing icon is generated to warn the user that only about 20 minutes of usable battery capacity remains.

2. Power To/From External Accessories

   The switched 7.5V also powers external accessories used with the radio. The voltage is picked up from the controller board and passed to the front cover/display flex via connector jack J701 pin 16 (OPT B+/BOOT SEL). The front cover/display flex then applies the voltage to pin 4 of the universal connector, where it is picked up by external accessories. Resistor R714, with a 1W power rating, provides current limiting to the external circuit to prevent internal damage should the external connector short.

The open architecture controller board uses Flash memory (U715) in place of conventional EPROMs. This allows the firmware to be reprogrammed through the side connector without opening the radio. The smart RIB box (SRIB) is used in conjunction with the RSS software program to perform the Flash reprogramming operation. While this occurs, the SRIB applies 12.7 V at different times to two of the radio side connector pins, 4 and 10. Pin 4 is the OPT B+/BOOT SEL pin. When 12.7 volts is applied to this pin, zener diode VR713 starts conducting and turns on both transistors contained in U703. The outputs of these transistors pull the MODA/MODB pins of U705 low and also control mux logic involving U709 to separate the microprocessor's SCI TX and RX paths, which are necessary for bootstrapping code into the µC during Flash reprogramming. Diode CR701 is needed to prevent current from flowing from the external 12.7 V source into the battery.

When 12.7 V is applied to pin 10 of the side connector, current flows through diode CR705 and approximately 12.0 V is presented to the Vpp pin of Flash memory (U715), which is required for reprogramming. Resistor R723 and zener diode VR715 prevent excess voltage from appearing at the input to U710-B6 when the 12.7 volts is applied.

3. Controller Board 5V Regulators

To reduce the possibility of digital noise coupling into the audio circuitry, the controller board uses separate analog and digital 5V supplies. The controller board regulated 5V for the digital circuitry (Vdd) is derived from a dedicated linear regulator IC (U708) which also provides a low voltage reset function. This device uses SW B+ as input and produces an output that is regulated to 5V ±0.1V. The low voltage error output (U708 pin 5) is used to hold the microprocessor (U705) RESET line low during power turn-on and turn-off conditions or when the battery is accidentally discharged to a very low voltage; this prevents the microprocessor from operating erratically during low voltage conditions.

The regulated analog 5V supply (Vaud) from audio PA U702 provides the operating voltage for audio IC U701. It is generated in conjunction with the external PNP pass transistor Q701. The circuit uses a negative feedback loop with an internal differential amplifier and a reference voltage inside U702. As the load on the 5V changes, the amplified error voltage is fed back to the base of transistor Q701 to keep the 5V regulated to a tolerance of ±0.25V.

III. VHF/UHF TRANSCEIVER

A. Frequency Generation Unit (FGU)

The frequency generation unit (FGU) consists of three major sections; the high stability reference oscillator (U203), the fractional-N synthesizer (U204,) and the VCO buffer (U201). A 5V regulator (U202), supplies power to the FGU. The synthesizer receives the 5V REG at U204, and applies it to a filtering circuit within the module and capacitor C253. The well filtered 5-volt output at U204 pin 19 is distributed to the TX and RX VCOs and the VCO buffer IC. The mixer LO injection signal and transmit frequency are generated by the RX VCO and TX VCO respectively. The RX VCO uses an external active device (Q202), whereas the TX VCO active device is a transistor inside the VCO buffer. The base and emitter connections of this internal transistor are pins 11 and 12 of U201.

The RX VCO is a Colpitts-type oscillator, with capacitors C235 and C236 providing feedback. The RX VCO transistor (Q202) is turned on when pin 38 of U204 switches from high to low. The RX VCO signal is received by the VCO buffer at U201 pin 9, where it is amplified by a buffer inside the IC. The amplified signal at pin 2 is routed through a low-pass filter (L201 and assocated capacitors) and injected as the first LO signal into the mixer (U2 pin 8). In the VCO buffer, the RX VCO signal (or the TX VCO signal during transmit) is also routed to an internal prescaler buffer. The buffered output at U201 pin 16 is applied to a low-pass filter (L205 and associated capacitors). After filtering, the signal is routed to a prescaler divider in the synthesizer at U204 pin 21.

The divide ratios for the prescaler circuits are determined from information stored in a codeplug, which is part of the microprocessor (U705). The microprocessor extracts data for the division ratio as determined by the position of the channel-select switch (S401), and busses the signal to a comparator in the synthesizer. A 16.8MHz reference oscillator, U203, applies the 16.8MHz signal to the synthesizer at U204 pin 14. The oscillator signal is divided into one of three pre-determined frequencies. A time-based algorithm is used to generate the fractional-N ratio.

If the two frequencies in the synthesizer's comparator differ, a control (error) voltage is produced. The phase detector error voltage (V control) at pin 31 and 33 of U204, is applied to the loop filter consisting of resistors R211, R212, and R213, and capacitors C244, C246, C247 and C275 . The filtered voltage alters the VCO frequency until the correct frequency is synthesized. The phase detector gain is set by components connected to U204 pins 28 and 29.

In the TX mode, U204 pin 38 goes high and U201 pin 14 goes low, which turns off transistor Q202 and turns on the internal TX VCO transistor in U204. The TX VCO feedback capacitors are C219 and C220. Varactor

diode CR203 sets the TX frequency while varactor CR202 is the TX modulation varactor. The modulation of the carrier is achieved by using a 2-port modulation technique. The modulation of low frequency tones such as DPL/TPL is achieved by injecting the tones into the A/D section of the fractional-N synthesizer. The digitized signal is modulated by the fractional-N divider, generating the required deviation. Modulation of the high frequency audio signals is achieved by modulating the varactor (CR203) through a frequency compensation network. Resistors R207 and R208 form a potential divider for the higher frequency audio signals.

In order to cover the very wide bandwidths, positive and negative V-control voltages are used. High control voltages are achieved using positive and negative multipliers. The positive voltage multiplier circuit consists of components CR204, C256, C257 and reservoir capacitor C258.The negative multiplier circuit consists of components CR205, CR206, C266, C267 and reservoir capacitor C254 in VHF and UHF radios. Out-of-phase clocks for the positive multiplier appear at U204 pins 9 and 10. Out-of-phase clocks for the negative multiplier appear at U204 pins 7 and 8, and only when the negative V-control is required (i.e., when the VCO frequency exceeds the crossover frequency). When the negative V-control is not required, transistor Q201 is turned on, and capacitor C259 discharges. The 13V supply generated by the positive multiplier is used to power up the phase detector circuitry. The negative V-control is applied to the anodes of the VCO varactors.

The TX VCO signal is amplified by an internal buffer in U201, routed through a low pass filter and routed to the TX PA module, U105 pin 1. The TX and RX VCOs and buffers are activated via a control signal from U204 pin 38.

The reference oscillator supplies a 16.8MHz clock to the synthesizer where it is divided down to either a 2.1MHz or a 2.4MHz clock. This divided-down clock is fed to the controller board ASF IC (U701), where it is further processed for internal use. Module U701 also use this signal to synthesize the microcomputer clock. The controller will program the synthesizer to provide 2.1MHz or 2.4MHz as required.

B. Antenna Switch

Two antenna switches are part of the radio circuitry. One of the switches (S101) is mechanical. It switches between the radio antenna and a remote antenna. Switching of S101 is accomplished by a plunger located on the accessory connector. With a remote antenna installed, continuity between the radio antenna and the RF input line (S101 pin 1 to pin 3) is broken; continuity is made from the remote antenna to the radio RF line (S101 pin 2 to pin 3). The second switch is a current device. It is a pair pair of diodes (CR108/CR109) that electronically steer RF between the receiver and the transmitter. In the transmit mode, RF is routed through transmit switching diode CR108, and sent to the antenna. In the receive mode, RF is received from the antenna, routed through receive switching diode CR109, and applied to the RF amplifier, U1. In transmit, bias current, sourced from U101 pin 21, is routed through L105, U104, CR108, and L122 in VHF and L105, CR108, and L122 in UHF. Sinking of the bias current is through the transmit ALC module, U101 pin 19. In the receive mode, bias current, sourced from SB+, is routed through Q107 (pin 3 to pin 2), L131 (VHF) or L123 (UHF), L121, CR109, and L122. Sinking of the bias current is through the 5-volt regulator, U103 pin 3.

C. Receiver Front End

The RF signal is received by the antenna and coupled through RF switch S101 and applied to a low-pass filter comprised of: VHF; L126, L127, L128, C130, C149, C150, and C151, or UHF; L126, L127, L128, C149, C150, and C151. The filtered RF signal is passed through the antenna switch (CR109) and applied to a bandpass filter comprised of: VHF; L11, L30 thru L35, CR6 thru CR9, C1, C2, and C3, or UHF; L30, L31, L32, L34, L35, CR6 thru CR9, C1, C2, and C3. The bandpass filter is tuned by applying a control voltage to the varactor diodes in the filter. (CR1-CR9 in VHF and CR6-CR9 in UHF.)

The bandpass filter is electronically tuned by the D/A IC (U102) which is controlled by the microcomputer.The D/A output range is extended through the use of a current mirror, transistor Q108 and associated resistors R115 and R116. When Q108 is turn on via R115, the D/A output is reduced due to the voltage drop across R116. Depending on the carrier frequency the microcomputer will turn on or off Q108. Wideband operation of the filter is achieved by retuning the bandpass filter across the band.

The output of the bandpass filter is applied to a wideband GaAs RF amplifier IC, U1 (RF AMP). Automatic gain control (AGC) is applied to the RF amplifier through an AGC network consisting of pin diode CR11, resistor R72 (VHF) or R52 (UHF), and choke L32(VHF) or L16 (UHF). The AGC control voltage is derived from pin 4 of the IF IC, U3. Bypassing is provided by capacitors C59 in UHF and C70 in VHF, while temperature compensation is provided by Schottky diode CR12 and R70 (VHF) or R51 (UHF). When a strong signal is received, the voltage at U3 pin 4 drops, causing current to flow from the receive 5-volt line (R5) through the pin diode (CR11). When this happens, the RF signal is shunted to ground via capacitor C16, in UHF and C71 in VHF thus reducing the amplitude of the RF signal applied to the 1st mixer. When the received RF signal is very weak, the voltage at U3 pin 4 rises and no current flows through CR11. The RF amplifier will then be at maximum gain. After being amplified by the RF AMP, the RF signal is further filtered by a second broad-band, fixed-tuned, bandpass filter consisting of C6, C7, C8,

C80, C86, C87, C88, C97, C99, L3, L4, L5, and L30 (VHF); or C4 thru C7, C88 thru C94, C99, and L11 thru L15 (UHF) to improve the spurious rejection.

Via a broadband 50-ohm transformer, T1, the filtered RF signal is routed to the input of a broadband mixer/buffer (U2). Mixer U2 uses GaAs FETs, in a double-balanced Gilbert Cell configuration. The RF signal is applied to the mixer at U2 pins 1 and 15. An injection signal (1st LO) of about -10dBm, supplied by the FGU, is applied to U2 pin 8. Mixing of the RF and the 1st LO results in an output signal which is the first IF frequency. The first IF frequency of VHF and UHF bands are 44.85 MHz and 73.35 MHz respectively. The 1st LO signal for VHF is 44.85 MHz higher than the carrier frequency while that for the UHF is 73.35 MHz lower than the carrier frequency. The 1st IF signal output, at U2 pins 4 and 6, is routed through transformer T2 and impedance matching components, and applied to a 2-pole crystal filter (FL1), which is the final stage of the receiver front end. The 2-pole crystal filter removes unwanted mixer products as the filtered IF signals being routed to the IF module, U3. Impedance matching between the output of the transformer (T2) and the input of the filter (FL1) is accomplished by capacitors C35 and C36 and inductor L20.

D. Receiver Back End

The output of crystal filter FL1 is matched to the input of IF buffer amplifier transistor Q4 by components C39, L22 and C38. Transistor Q4 is biased by the voltage level on U2 pin 3. The IF frequency on the collector of Q4 is applied to U3 pin 2, where it is down converted, amplified, filtered, and demodulated, to produce the recovered audio at U3 pin 28. This IF IC is electronically programmable, and the amount of filtering (which is dependent on the radio channel spacing) is controlled by the microcomputer. Additional filtering, which used to be provided externally by conventional ceramic filters, is replaced by internal filters in the IF module. The IF IC uses a type of direct conversion process where the second LO frequency is very close to the first IF frequency. The IF IC synthesizes the second LO and phase locks the VCO to track the first IF frequency.

In the absence of an IF signal, the VCO will "hunt," or its frequency will vary about a frequency close to the IF frequency. When an IF signal is received, the VCO will lock onto the IF signal. The 2nd LO/VCO is a Colpitts oscillator built around transistor Q1. The VCO has a varactor diode, CR5, to adjust the VCO frequency. The control signal for the varactor is derived from a loop filter consisting of C52, C53, and R16.

The IF IC (U3) performs several other functions. It provides a received signal strength indicator (RSSI) and a squelch output. The RSSI is a dc voltage monitored by the microcomputer and used as a peak indicator during bench tuning of the receiver front-end varactor filter. The RSSI dc voltage is sent from U3 pin 9 to connector jack J301 pin 11, where it is routed through the jumper flex (P301 pin 11 to P704 pin 11) and applied to the controller board. In the controller board the RSSI is routed through the ASF IC (U701 pin 11 to U701 pin 41), and applied to the front cover flex at J701 pin 21.Via the front cover flex, the RSSI voltage reaches its destination, at the universal connector at P403 pin 7 as RTS. The squelch output of U3, on pin 29, is a high-frequency audio signal. The squelch signal is routed to shaping and detection circuits within U701 on the controller board, for use in other parts of the radio. The IF module (U3) also monitors the strength of the received signal, to provide an AGC voltage at pin 4, which is then fed to the RF amplifier AGC circuit. Inductor L23 and capacitor C70 prevent any IF signal from leaking back to the front-end circuits.

E. Transmitter

The transmitter consists of three major sections:

- Harmonic Filter
- RF Power Amplifier Module
- ALC Circuits

1. Harmonic Filter

   RF from the Power Amplifier (PA) module, U105 is routed through the coupler (U104), passed through the transmit antenna switch (CR108), and applied to a harmonic filtering network. The harmonic filtering circuit is comprised of the following components: L126, L127, L128, C149, C150, and C151 (for VHF models); or L126, L127, L128, C129, C130 C149, C150, and C151 (for UHF models). Resistor R128 (UHF) or R117 (VHF) provides a current limited 5V to P402 for mobile vehicular adapter (MTVA) applications.

2. RF Power Amplifier Module

   The RF power amplifier module (U105) is a wideband multi-stage amplifier (3 stages for the VHF models and 4 stages for the UHF models). Nominal input and output impedance of U105 is 50 ohms. The dc bias for U105 is on pins 2, 4, 5. In the transmit mode, the voltage on U105 pins 2 and 4 (close to the B+ level) is obtained via switching transistor Q101. Transistor Q101 receives its control base signal as follows:

   - the microcomputer keys the D/A IC to produce a ready signal at U102 pin 3
   - the ready signal at U102 pin 3 is applied to the TX ALC IC at U101 pin 14 (5V)
   - the synthesizer sends a LOC signal to the TX ALC IC (U204 pin 40 to U101 pin 16

   When the LOC signal and the ready signal are both received, the TX ALC IC (pin 13) sends a control signal to turn on transistor Q101.

3. ALC Circuits

Coupler module U104 samples the forward power and the reverse power of the PA output voltage. Reverse power is present when there is other than 50 ohms impedance at the antenna port. Sampling is achieved by coupling some of the forward and/or reverse power, and apply it to CR102(VHF) or CR101(UHF) and CR103 for rectification and summing. The resultant dc signal is then applied to the TX ALC IC (U101 pin 2) as RFDET to be used as an RF strength indicator.

The transmit ALC circuit, built around U101, is the heart of the power control loop. Circuits in the TX ALC module compare the signals at U101 pins 2 and 7. The resultant signal, C BIAS, at U101 pin 4 is applied to the base of transistor Q110. In response to the base drive, transistor Q110 varies the dc control voltages applied to the RF PA at U105 pin 3, thus controlling the RF power of module, U105.

Thermistor RT101 senses the temperature of the TX ALC IC. If an abnormal operating condition exists, which causes the PA slab temperature to rise to an unacceptable level, the thermistor forces the ALC to reduce the set power.

IV. 800/900MHz TRANSCEIVER BOARD

A. Frequency Synthesis

The complete synthesizer subsystem consists of the reference oscillator (U203), the voltage controlled oscillator (VCO), U205, a buffer IC (U201), and the synthesizer U204).

The reference oscillator contains a temperature-compensated 16.8 MHz crystal. This oscillator is digitally tuned and contains a temperature-referenced 5-bit analog-to-digital (A/D) converter. The output of the oscillator (pin 10 on U203) is applied to pin 14 (XTAL1) on U204 via capacitor C284 and resistor R222.

Module U205 is the voltage controlled oscillator, which is varactor tuned; that is, as the voltage (2-11V) being applied to pins 1 and 7 of the VCO varies, so does the varactor's capacitance, thereby changing the VCO's output frequency. The 800MHz VCO is a dual-range oscillator that covers the 806-825MHz and the 851-870MHz frequency bands. The low-band VCO (777-825MHz) provides the first LO injection frequencies (777-797MHz) that will be 73.35MHz below the carrier frequency. In addition, when the radio is operated through a repeater, the low band VCO will generate the transmit frequencies (806-825MHz) that will be 45MHz below the receiver frequencies. The low-band VCO is selected by pulling pin 3 high and pin 8 low on U205. When radio-to-radio or talk-around operation is necessary, the high band VCO (851-870MHz) is selected. This is accomplished by pulling pin 3 low and pin 8 high on U205.

The 900MHz VCO is also a dual-range oscillator that covers the 896-902MHz and the 935-941MHz frequency bands. The low-band VCO (861-902MHz) provides the first LO injection frequencies (861-867MHz) that will be 73.35MHz below the carrier frequency. In addition, when the radio is operated through a repeater, the low-band VCO will generate the transmit frequencies (896-902MHz) that will be 39MHz below the receiver frequencies. When talk-around operation is necessary the high-band VCO (935-941MHz) is selected.

The buffer IC, U201, includes a TX, RX, and prescaler buffer whose main purpose is to individually maintain a constant output and provide isolation. The TX buffer is chosen by setting pin 7 of U201 high; the RX buffer is chosen by setting pin 7 of U201 low. The prescaler buffer will always be on. In order to select the proper combination of VCO and buffer, the following conditions must be true at pin 6 of U201 (or pin 38 of U204) and pin 7 of U201 (or pin 39 of U204). For the first LO injection frequencies 861-867MHz (A), pins 6 and 7 must both be low; for the TX repeater frequencies 896-902 MHz (B) pins 6 and 7 must both be high, and for talk-around TX frequencies 935-941 MHz (C) pin 6 must be low while pin 7 must be high.

(A) = 777-797MHz for 800MHz; 861-867MHz for 900MHz
(B) = 804-825MHz for 800MHz; 896-902MHz for 900MHz
(C) = 851-870MHz for 800MHz;935-941MHz for 900MHz

The synthesizer IC, U201 consists of a prescaler, a programmable loop divider, a divider control logic, a phase detector, a charge pump, an A/D converter for low frequency digital modulation, a balance attenuator to balance the high frequency analog modulation to the low frequency digital modulation, a 13V positive-voltage multiplier, a serial interface for control, and finally a filter for the regulated five volts. This filtered five volts is present at pin 19 of U204, pin 9 of U205, and pins 2,3,4, and 15 of U201. It is also applied directly to resistors R214, R215, and R220. Additionally, the 13V, being generated by the positive voltage multiplier circuitry, should be present at pin 35 of U204. The serial interface (SRL) is connected to the microprocessor via the data line (pin 2 of U204), clock line (pin 3 of U204), and chip enable line (pin 4 of U204).

The complete synthesizer subsystem works as follows. The output of the VCO, pin 4 on U205, is fed into the RF input port (pin 9) of U201. In the TX mode, the RF signal will be present at pin 4 of U201. On the other hand, in the RX mode, the RF signal will be present at pin 3 of U201. The output of the prescaler buffer, pin 15 on U201, is applied to the PREIN port (pin 21) of U204. The prescaler in U204 is a dual-modulus type with selectable divider ratios. This divider ratio is controlled by the loop divider, which in turn receives its inputs via

the SRL. The loop divider adds or subtracts phase to the prescaler divider by changing the divide ratio via the modulus control line. The output of the prescaler is then applied to the loop divider. The output of the loop divider is then applied to the phase detector. The phase detector will then compare the loop divider's output signal with the signal from U203 (that is divided down after it is applied to pin 14 of U204). The result of the signal comparison is a pulsed dc signal which is applied to the charge pump. The charge pump outputs a current that will be present at pin 32 of U204. The loop filter (which consists of capacitors C237, C238, C246, C275, C239, and C240, and resistors R212, R211, R213, and R241) will transform this current into a voltage that will be applied to pins 1 and 7 of U205, and alter the VCO's output frequency.

In order to modulate the PLL, the two-spot modulation method is utilized. The analog modulating signal is applied to the A/D converter as well as the balance attenuator, via U204 pin 5. The A/D converter converts the low frequency analog modulating signal into a digital code that is applied to the loop divider, thereby causing the carrier to deviate. The balance attenuator is used to adjust the VCO's deviation sensitivity to high frequency modulating signals.

B. Antenna Switch

Switching between the standard and external antenna ports is accomplished with switch S101 which is actuated by a plunger located on the accessory connector.

An electronic PIN diode switch steers RF between the receiver and transmitter. The common node of the switch is at capacitor C151. In the transmit mode, RF is routed to the anode of diode CR108. In receive mode, RF is routed to pin 1 of U4. In transmit, bias current sourced from U101 pin 21, is routed through PIN diodes CR108 and CR109, biasing them to a low impedance state. Bias current returns to ground through U101 pin 20. In receive, U101 pin 21 is pulled down to ground and pin 20 is pulled up to B+, reverse biasing diodes CR108 and CR109 to a high impedance.

C. Receiver Front End

For the purposes of this discussion, the receiver front end is defined to be the circuitry from the antenna switch to the output of the IF crystal filter. The 800 MHz and 900MHz front end is designed to convert the received RF signal to the 1st IF frequency of 73.35MHz, while at the same time providing for spurious immunity and adjacent channel selectivity. A review of the interstage components of the front end will now be presented with emphasis on troubleshooting considerations.

The received RF signal is passed through the antenna switch input matching components C151, L127, tank components C149 & L126 (which are anti-resonant at the radios transmitter frequencies), and output matching components C141 and L30. Both pin diodes CR109 and CR108 must be back biased to properly route the received signal.

The stage following the antenna switch is a 50-ohm, inter-digitated, 3-pole, stripline preselector (U4). The preselector is positioned after the antenna switch to provide the receiver preamp some protection to strong signal, out-of-band signals.

After the preselector (U4), the received signal is processed through the receiver preamp, U1. The preamp is a dual-gate GaAs MESFET transistor which has been internally biased for optimum IM, NF, and gain performance. Components L32 and L34 match the input (gate 1) of the amp to the first preselector, while at the same time connecting gate 1 to ground potential. The output (drain) of the amp is pin 3 and is matched to the subsequent receiver stage via components L10, C4 and C88. A supply voltage of 5Vdc is provided to pin 3 via an RF choke L8 and bypass C31. The 5 volt supply is also present at pin 4 which connects to a voltage divider network that biases gate 2 (pin 5) to a predefined quiescent voltage of 1.2Vdc. R27 and C11 are connected to pin 5 to provide amp stability. The FET source (pin 7) is internally biased at 0.55 to 0.7Vdc for proper operation with bypass capacitors C13 and C72 connected to the same node.

The output of the amp is matched to a second 3-pole preselector (U5) of the type previously discussed. The subsequent stage in the receiver chain is the 1st mixer U2, which uses low-side injection to convert the RF carrier to an intermediate frequency (IF) of 73.35MHz. Since low-side injection is used, the LO frequency is offset below the RF carrier by 73.35MHz, or Flo = Frf - 73.35MHz. The mixer utilizes GaAs FETs in a double balanced Gilbert Cell configuration. The LO port (pin 8) incorporates an internal buffer and a phase shift network to eliminate the need for a LO transformer. The LO buffer bypass capacitors C82, C90 and C91 are connected to pin 10 of U2, and should exhibit a nominal dc voltage of 1.2 to 1.4Vdc. Pin 11 of U2 is LO buffer Vdd (5Vdc) with associated bypass capacitors C19 and C92 connected to the same node. An internal voltage divider network within the LO buffer is bypassed to virtual ground at pin 12 of U2 via bypass C84. The mixer's LO port is matched to the radio's PLL by a capacitive tap, C204 and C206. A balun transformer (T1) is used to couple RF signal into the mixer. The primary of T1 is matched to the preceding stage by capacitor C7, with C98 providing a dc block to ground. The secondary of T1 provides a differential output, with a 180° phase differential being achieved by setting the secondary center tap to virtual ground using bypass capacitors C89, C83 and C86. The secondary of transformer T1 is connected to pins 1 and 15 of the mixer IC, which drives the source leg of dual FETs used to toggle the paralleled differential amplifier configuration within the Gilbert Cell.

The final stage in the receiver front end is a 2-pole crystal filter, FL12. The crystal filter provides some of the receiver's adjacent channel selectivity. The receiver's backend IF IC (U3) provides most of the adjacent channel selectivity, using integrated baseband low-pass filters. The input to the crystal filter is matched to the 1st mixer using components L36, L20, C35 and C36. The output of the crystal filter is matched to pin 2 of the IF IC using inductor L22, and a capacitive tap C38 and C39.

D. Receiver Back End

The IF frequency is applied to the IF IC (U3), where it is down converted, amplified, filtered, and demodulated to produce the recovered audio. This IF IC is electronically programmable and the amount of filtering (which is dependent on the radio channel spacing) is controlled by the microprocessor. Additional filtering, which used to be provided externally by conventional ceramic filters, is replaced by internal filters in the IF IC. The IF IC uses a type of direct conversion process where the second LO frequency is very close to the IF frequency. The IF IC controls the second LO VCO and causes the VCO to track the first IF frequency, producing a phased lock operation. The IF IC also provides a recovered signal strength indicator (RSSI) and squelch output for use in other parts of the radio.

E. Transmitter

The 800MHz and 900MHz RF PAs are 5-stage amplifiers. Both RF power amplifiers have nominal input and output impedances of 50 ohms.

An RF input drive level of approximately +3 dBm, supplied from the VCO buffer IC, U201 is applied to pin 1 of U105. The dc bias for the internal stages of U105 is applied to pins 2,5,and 6 of the module. Pins 2 and 5 being switched through Q101 and pin 6 being unswitched B+ to the final amplifier stage. Power control is achieved through the varying of the dc bias to pins 3 and 4, the third and fourth amplifier stages of the module. The amplified RF signal leaves the PA module via pin 7 and is applied to the directional coupler, U104.

The purpose of U104 is to sample both the forward power and the reverse power. The reverse power will be present when there is other than a 50-ohm load at the antenna port. The sampling will be achieved by coupling some of the reflected power, forward and/or reverse, to a coupled leg on the coupler. The sampled RF signals are applied to diode CR101 for rectification and summing. The resultant dc signal is applied to the ALC IC (U101 pin 2) as RFDET to be used as an strength indicator of the RF signal being passed through the directional coupler, U104.

The transmit ALC IC, U101, is the heart of the power control loop. The REF V line (U101 pin 7), a dc signal supplied from the D/A IC (U102), and the RF DET signal described earlier, are compared internally in the ALC IC to determine the amount of C BIAS, pin 4, to be applied to the base of transistor Q110. Transistor Q110 responds to the base drive level by varying the dc control voltages applied to pin 3 and 4 of the RF PA, controlling the RF power level of module, U105. The ALC IC also controls the base switching to transistor Q101 via pin 12, BIAS.

The D/A IC, U102, controls the dc switching of the transceiver board. Its outputs, SC1 and SC3, pins 12 and 14 respectively, control transistor Q108, which then supplies TX 5V and RX 5V to the transceiver board. The D/A also supplies the dc bias to the detector diode (CR101) via pin 7, and the REF V signal to the ALC IC, U101.

V. CLOSED ARCHITECTURE CONTROLLER

Since the controller is the central interface between the various subsystems of the radio, and because of the controllers complexity, this section will be divided into two areas of discussion, the microcomputer and its functions, and the controller board circuit operation.

A. Microcomputer (U705)

The heart of the HT 1000 controller consists of a new generation Motorola microcomputer, U705. The microcomputer consists of 640 bytes of EEPROM, 760 bytes of RAM, and 24K of ROM. It operates in single-chip mode. The microcomputer is powered by a regulated 5V output from voltage regulator U709. The microcomputer clock is generated by the ASFIC, U701, which has a built in programmable clock synthesizer.

1. Functions

   The microcomputer, has two basic functions: interfacing to the outside world and controlling the internal workings of the radio. It interfaces directly to the side buttons, PTT, rotary switch, toggle switch, and 13-pin side connector. It is constantly monitoring a numerous amount of inputs, interpreting any changes that may be occurring, and responding with commands that control the rest of the radio. Some functions that it performs include:

   - loading the synthesizer with the desired RF frequency,
   - turning the RF PA on or off,
   - turning the microphone and speaker on or off,
   - enabling and disabling audio and data paths, and
   - generating tones.

   Operations and operating conditions within the radio are interpreted by the microcomputer and fed back to the operator as audible (alert tone) indications of the radio's immediate status.

2. Microcomputer Clock Synthesizer

   Upon power-up, and assuming that the ASF IC receives a proper 2.1MHz input at U701 pin 33 (which comes from the transceiver board), the ASF IC outputs a 3.6864MHz CMOS square wave on U701 pin 35. This UP CLK signal connects to the input of the microcomputer (U705 pin 77) as EXTAL. The microcomputer operates at 1/4 of this frequency, which in this case computes to 921.6KHz.

   After initialization, upon power-up, the microcomputer programs the ASF IC to change the E-clock to 1.9872 MHz. Therefore, soon after the controller is powered up, serial data is sent to the ASF IC on signal line U701 pin 32, while select line U701 pin 30 is held low. The result is a 1.9872MHz clock signal (4x 1.9872MHz) on U701 pin 35.

3. SB9600 Serial Interface

   The radio uses a proprietary multiprocessor serial protocol known as SB9600. This protocol allows the microcomputer in the system to interface with an external personal computer (PC) for RSS programming, a remote hand-held mic, or a vehicular adapter.

   From a hardware standpoint, the external interface is the universal side connector, BUSY and DATA lines (P403 pins 9 and 13 respectively). The DATA signal is a bidirectional 0-5V RS-232 line that uses U705's integrated RS-232 asynchronous serial communication interface (SCI) peripheral. The SCI TX line is U705-PD1 and the SCI RX line is U705-PD0. The SCI TX line and the SCI RX line are connected together, thus providing the DATA signal, which is routed to the controller connector jack, J701 pin 26. The BUSY signal (at U705 pin 8, PA3) is an active-high bidirectional signal that is normally pulled down by 10K resistor R737. The BUSY signal is routed to the controller connector jack, J701 pin 22.

   A typical usage of the SB9600 interface occurs when using a PC to run the RSS software package and the radio interface box (RIB) to program the radio's codeplug. When the PC sends a command or data to the radio, observe the SCI RX line (U705 pin 82, PD0) toggling at a 9600 baud rate and the BUSY line going high when data is actually being sent. After the data transfer is complete, the busy line should idle low and the LH DATA line should idle high. The controller board also sends a power-up status message when it is first turned on. The SB9600 data being sent from the radio can be observed within a few msec. after power-up.

4. SPI Interface

   The microcomputer communicates to several ICs and modules through a dedicated on-chip SPI port, which consists of a transmit data line (U705 pin 1, PD3), a receive data line (U705 pin 84, PD2), and a clock line (U705 pin 2, PD4). In addition, each IC that can be accessed by the microcomputer, using the SPI, has a select line associated with it. The programmable ICs or circuits and their associated select lines are:

   - ASF IC (U701) - select line at U701 pin 30
   - transceiver board reference oscillator (U203) - select line at U203 pin 24
   - transceiver board synthesizer (U204) - select line at U204 pin 4
   - transceiver board I-F (U3) - select line at U3 pin 21
   - transceiver board D/A IC (U102) - select line at U102 pin 16

   The select lines for all of the SPI devices listed are active low; i.e., the select line goes low when the associated device is being programmed.

5. Option Select Lines

   The two option select lines, OPT SEL 1 and OPT SEL 2 (P403 pins 1 and 5, respectively), are used to identify the presence of external accessories and also to key up the radio with an external microphone. Table 1 shows the function and the two associated signal states sensed by the microcomputer at U705 pins 38 and 37. Both signals have pull-up resistors inside the microcomputer, so that if no external device is connected to these pins, they will be at a logic high level and the radio will be in the normal mode; i.e., internal speaker and microphone will be used.

   Radio frequency power will always be routed to the internal antenna port, unless a side connector is installed that mechanically activates RF switch S101, which redirects power to the external antenna port. The microcomputer has no knowledge or control of which port RF energy is being directed. An external PTT [OPT SEL 1 = 0 (low), OPT SEL 2 = 0 (low)], will cause the external mic audio port to be activated, but the RF could be routed through either RF port.

Table 1. Option Select Definition

OPT SEL 1	OPT SEL 2	FUNCTION
High	High	Normal
Low	High	External Speaker
Low	Low	External PTT
High	Low	Man Down

6. LED Control

   The bicolor LED (CR702A and CR702B) is activated by microcomputer U705 in conjunction with the

dual NPN transistor IC, U704. When either of the outputs (U705 pin 66, PC1 or U705 pin 65, PC0) is at a logic high, the corresponding output of U704 (pin 3 for the green LED, pin 6 for the red) is at approximately 4.3volts. Note that it is possible to have both LED outputs on simultaneously, in which case the LED emits an orange/yellow light.

B. Controller Board Circuit Operation

The circuits considered here are those circuits that involve:

- the transmit audio path between the microphone and the transmit RF section,
- the transmit data path between the microcomputer and the transmit RF section,
- the receive audio path between the receive RF section and the speaker,
- the receive data path between the receive RF section and the microcomputer, and
- the alert tone path between the microcomputer and the speaker.

The transmit and receive audio paths are disabled in the standby mode and selectively enabled by the microcomputer when the radio transmits or receives a signal. Also, there are minor differences in the functioning of both paths depending on whether an internal or external (accessory) speaker/microphone is being used.

1. Transmit Audio Circuits

   There are three major circuits in the transmit audio path. Some require enable lines and some are active devices that are always operating. When the PTT is depressed, the radio will monitor the channel for traffic (smart PTT). If the channel is not busy, the microcomputer will enable the path between the microphone and the RF section.

   The microphone in the front cover (internal mic) and remote microphone (external mic) are of the FET electric type. They require a dc biasing voltage, provided by resistors R701 and R756, respectively. The INT MIC audio is routed to module U701 pin 2. The EXT MIC audio is routed to module U701 pin 54. Logic inside the ASF IC selects one of the signals for amplification and processing.

   a. Internal Microphone Path

      The internal microphone (MK401) is located on the front cover of the radio and is connected to the controller board via connector plug P701 pin7. On the controller, from connector jack J701 pin 7, the audio signal is routed to resistors R701 and R703. Resistor R701 performs dc biasing and resistor R703 provides input protection for the CMOS amplifier input. Filter capacitor C703 provides low-pass filtering to eliminate frequency components above 3KHz, and capacitors C706 and C779 serve as dc blocking components. The high-pass filter formed by capacitor C779 and resistor R704 attenuates objectionable low-frequency audio components of speech. The audio signal is passed on to the ASF IC, U701 pin 2.

   b. External Microphone Path

      The external microphone signal enters the radio via universal connector P403 pin 3, and is connected to the controller board through connectors P701/J701 pin 14. The external audio signal is routed through a filtering circuit composed of L701, C721, R702, and C702, through dc blocking capacitor C705, and passed to the ASF IC, U701 pin 54. Resistor R756 provides dc bias for the stage.

   c. PTT Sensing and Transmit Audio Processing

      Depressing the internal PTT switch (S406) provides a ground path for the microcomputer via the controls flex to controller connector P703/J703 pin 1 and an internal pull-up resistor at the input of U705 pin 61, PF2. Depressing an external PTT switch provides a ground path for both input lines (OPT SEL 1 and OPT SEL 2, via the universal connector (P403 pins 1 and 5 respectively). The ground is read by the microcomputer at U705 pin 38 (PG5) and U705 pin 37, (PG6). When either PTT is sensed (internal or external), the microcomputer configures the ASF IC for the proper audio path. Inside the ASF IC, the audio input signal is amplified, filtered to eliminate components outside the 300-3000Hz voice band, pre-emphasized, and limited. The limited microphone audio is routed through a summer circuit, which adds PL or DPL sub-audio band modulation, and then routed to a splatter filter to eliminate high frequency spectral components generated by the limiter. After the splatter filter, the audio is routed to two modulation attenuators, which are tuned for the proper amount of FM deviation. The transmit audio signal emerges from the ASF IC at U701 pin 13, and is dc coupled to the synthesizer (U204 pin 5) on the transceiver board through connector jack J704 pin3.

2. Transmit Data Circuits

   There are three major types of transmit data: sub-audible data (PL/DPL), DTMF data for telephone communication, and MDC data for use in Motorola proprietary MDC systems. The deviation levels of the latter two types are tuned by a 5-bit digital attenuator inside the ASF IC. For each data type and each bandsplit, there is a distinct set of tuning values programmed into the ASF IC before the data can be generated and transmitted.

a. Sub-audible Data (PL/DPL)

Sub-audible data is composed of low-frequency PL and DPL waveforms for conventional operation. Although it is referred to as “sub-audible data,” the actual frequency spectrum of these waveforms may be as high as 250 Hz, which is audible to the human ear. However, the radio receiver filters out any audio below 300 Hz, so these tones are never heard in the actual system.

Only one type of sub-audible data can be generated by U705 at any one time. The process is as follows. Using the SPI, the microcomputer programs the ASF IC to set up the proper low-speed data deviation and select the PL or DPL filters. The microcomputer then generates and produces a square wave at U705 pin 6, PA5, which strobes the ASF IC PL/DPL encode input at U701 pin 40. Module U701 reacts to the strobe input by generating a staircase approximation to the PL sine wave or the DPL data pattern. This internal waveform is low-pass filtered and summed with voice or data. The resulting waveform appears at U701 pin 13, VCO ATN, where it is sent to the transceiver board as previously described for transmit audio.

b. DTMF Data

DTMF data is a dual-tone waveform used during phone interconnect operation. There are seven frequencies; four in the low group (697-941Hz) and three in the high group (1209-1477Hz). The high-group tone is generated by the microcomputer (U705 at pin 22, PH0), strobing the ASF IC (U701 at pin 29) at six times the tone frequency for tones lower than 1440Hz, or twice the frequency for tones higher than 1440Hz. The low-group tone is generated by the microcomputer (U705 pin 23, PH1) strobing the ASF IC (U701 pin 28) at six times the tone frequency. Circuits inside module U701 sum the low-group and high-group tones (with the amplitude of the high-group tone being approximately 2db greater than that of the low-group tone) and send the summed signal through a pre-emphasis network. The resultant signal is routed through a summer and splatter filter. After filtering, the signal is routed through modulation attenuators and sent from the ASF IC to the transceiver board. The signal path is from U701 pin 13 through the controller/jumper flex connector (J704/P704 pin 3), and through the jumper flex/transceiver board connector (P301/J301 pin 3) to the RF synthesizer (U204). The input signal is VCO MOD.

c. MDC Data

The MDC signal follows exactly the same path as the DTMF high group tone. MDC data utilizes MSK modulation, in which a logic zero is represented by one cycle of a 1200Hz sine wave, and a logic one is represented by 1-1/2 cycles of an 1800Hz sine wave. To generate the data, the microcomputer first programs the ASF IC (U701) to the proper filter and gain settings. It then begins strobing module U701 pin 29 (TRK CLK IN) with a square wave (from U705 pin 22, PH0) at the same baud rate as the data. The output waveform from U701 is fed to a post-limiter, to a summer block, and then to a splatter filter. The resultant signal is routed through modulation attenuators and sent from the ASFIC to the transceiver board using the same signal path as the DTMF data described in the previous paragraph.

3. Receive Audio Circuits

The major circuits in the receive audio path are the ASF IC (U701) and the audio PA (U706). The ASF IC is an SPI programmable device, while the audio PA has direct control lines.

The radio’s RF circuits are constantly producing an output at the discriminator. In the conventional standby mode, the radio’s receiver is always monitoring the squelch line and/or sub-audible data. The raw discriminator input signal (DISC) from the transceiver board enters the controller board on connector jack J704 pin 10. In addition to the raw discriminator signal, the transceiver board’s IF IC also provides a pre-filtered version of the discriminator signal, SQ OUT, that is dedicated to the ASFIC’s squelch-detect circuitry. The SQ OUT signal enters the controller board via connector jack J704 pin12 and is routed to the ASF IC, U701 pin 14. When the microcomputer is satisfied that it has received the proper data or signal type for unsquelching, it sets up the receive audio path and sends data for the ASF IC (U701) to process.

a. U701 Audio Processing and Digital Volume Control

The signal enters the ASF IC (U701) pin 16 for further processing. Inside the IC, the signal first passes through a low-pass filter to remove any frequency components above 3000 Hz, and then a high-pass filter to strip off any sub-audible data below 300 Hz. Next, the recovered audio passes through a de-emphasis filter to reduce the effects of FM noise. Finally, the IC amplifies the audio and passes it through an 8-bit programmable attenuator, whose level is set in accordance with the voltage sensed on the volume potentiometer, which is connected to

U705 pin 51, PE1. After passing through the 8-bit digital attenuator, the audio goes to a buffer amplifier and exits the module at U701 pin 21 (RX AUD OUT), where it is routed to audio PA module U706 (pin 8).

b. Differential Speaker Audio Amplification

The final stage in the receive path is the audio amplifiers that drive either the internal or external speakers. Each speaker is driven using a dual-amplifier arrangement. Since one amplifier can be shared as common between the two speakers, only three total amplifiers are needed inside the audio PA IC, U706.The audio signal is coupled into the amplifiers on U706 pin 8, AUD IN.

There are two enable lines controlling the three audio amplifies in module U706. They are the internal enable (INT EN) line and the power amplifier enable (PA EN) line. The INT EN input at U706 pin 21, which is used to control the phase of the internal or external amplifier, comes from U701 pin 43. The PA EN input at U706 pin 20, which enables all three amplifiers, comes from U701 pin 44. The INT EN line is active-low, while the PA EN line is active-high. The microcomputer determines which speaker that audio should be routed to (internal or external) by reading option select lines 1 and 2 (OPT SEL 1 and OPT SEL 2) at pins 1 and 5 of the universal connector, P403. If the microcomputer senses a vehicular adapter connected to the radio (which is identified by having a diode from OPT SEL 2 to OPT SEL 1, with the anode at OPT SEL 2), and the radio is in receive mode, the audio will be directed to the external speaker at P403 pins 2 and 6. The audio is set at a fixed level, independent of the radio volume pot setting. When the receive path is enabled, all three amplifiers in U706 are turned on. If the internal speaker amplifier is selected, then its output is 180 degrees out of phase with that of the common amplifier. The result at the internal speaker is a signal twice as large as either amplifier's output, while the external amplifier is in phase with the common amplifier; the result at the external speaker is no signal. The reverse is true if the external speaker is selected. The nominal voltage for rated audio is 3.74Vrms, and the nominal audio input to U706 is 88.7mVrms, when rated audio output is obtained.

4. Receive Data Circuits

The ASF IC (U701) is used to decode all receive data, which includes PL, DPL and MDC. The decode process for each data type typically involves low-pass or band-pass filtering, signal amplification, and routing the signal to a comparator, which outputs a logic zero or a logic one signal. The discriminator output from the transceiver board is routed to U701 pin 15 through coupling capacitor C710. Inside module U701, the data is filtered according to the data type [high-speed (HS) data or low-speed (LS) data], then hard-limited to a 0-5V digital level. The high-speed data output (MDC) appears at U701 pin 23, where it interconnects with the microcomputer, U705 pin 11, PA0. The low-speed limited data output (PL, DPL) appears at U701 pin 48, where it interconnects with U705 pin 10, PA1. If, for example, the radio is receiving 192.8 Hz PL, the discriminator should contain a 192.8 Hz sine wave at about 53 mVrms, and the limited PL output should be a 192.8 Hz square wave. While the radio is decoding PL, DPL, the microcomputer also outputs a sampling waveform on U705 pin 6, PA5, which is routed to U701 pin 40. The same line used to generate transmit PL or DPL data. This sampling waveform is a square wave between 1000 and 2000 Hz.

5. Alert Tone Circuits

When the microcomputer gives the operator feedback, radio status (low battery condition, circuit failures, etc.), it sends an alert tone to the speaker. It does so by sending data to ASF IC U701, which sets up the audio path to the speaker for alert tones. The alert tone itself can be generated in one of two ways: internally by the ASFIC, or externally using the microcomputer and the ASFIC. The allowable internal alert tones are 300, 900, and 1800 Hz. For external alert tones, the microcomputer can generate any tone within the 100-3000 Hz audio band. This is accomplished by the microcomputer toggling the output line U705 pin 5 (PA6) which is also the same line used to generate low-group DTMF data. Inside the ASF IC, the signal is routed to the external input of the alert tone generator; the output of the generator is summed into the audio chain after the RX audio de-emphasis circuit. Inside module U701, the tone is amplified, filtered, and passed through the 8-bit digital volume attenuator. The tone signal, from ASF IC U701 pin 21, is then routed to the audio PA the same as receive audio.

VI. OPEN ARCHITECTURE CONTROLLER

The open architecture controller consists of:

- U705, a new generation Motorola microprocessor;
- U710, a custom gate array;
- U715, normally a 256k or 512k memory;
- U714, a 32K static RAM; and
- U713, an EEPROM which could be 8K or 32k.

All of these devices are powered by regulated 5 volts provided by voltage regulator U708. In addition to

the external memory devices, U705 has 1k of RAM and 512 bytes of EEPROM on chip. Miscellaneous logic and switching functions are provided by U703, U709, and U711.

Since the controller is the central interface between the various subsystems of the radio, and because of the controllers complexity, this section will be divided into two areas of discussion, the microcomputer and its associated circuits, and the controller board's circuit operation.

A. Microprocessor (U705) and Associated Circuits

1. Functions

   The microprocessor, in conjunction with the SLIC gate array (U710) (which can actually be considered an extension of the microprocessor), has two basic functions: interfacing to the outside world and controlling the internal workings of the radio. The microprocessor interfaces directly to the keypad, display, side buttons, PTT, rotary switch, battery voltage indicator, toggle switch, and 13-pin universal connector. The microprocessor constantly monitors these inputs and interprets any changes into commands that control the rest of the radio. Some control functions it performs include loading the synthesizer with the desired RF frequency, turning the RF PA on or off, turning the microphone and speaker on or off, enabling and disabling audio and data paths, and generating tones. Operations and operating conditions within the radio are interpreted by the microprocessor and fed back to the operator as visible (the display) or audible (alert tone) indications of current status.

2. Normal Operation

   The regulated 5V output from U708 powers the microprocessor (U705) and the rest of the digital ICs. The controller's clock is generated by the ASF IC, U701, which has a built in programmable clock synthesizer.

3. Clock Synthesizer

   Upon power-up, and assuming that the ASF IC receives a proper 2.1MHz input on U701-E1 (which comes from the transceiver board), the ASF IC outputs a 3.6864MHz CMOS square wave (0-5Vpp logic) on U701-D1, which connects to the EXTAL input of the microprocessor, U705-A6. The microprocessor operates at 1/4 of this frequency, which in this case computes to 921.6 kHz. In particular, the E clock output (pin U705-A5) will be a 50% duty cycle square wave at this frequency, and will control all bus timing accesses. The clock signal is also routed to the SLIC (U710-A4).

   After initialization, and upon power-up, the microprocessor reprograms the ASF IC to change the E-clock to either 1.8432MHz or 3.6864MHz. Therefore, soon after the controller is powered up, serial data is being sent to the ASF IC on signal lines U701-E3 and U701-F1. The ASF IC select line U701-F2 is held low, and the UP CLK signal from U701-D1 should be 4 x 1.8432MHz (=7.3728MHz) or 4 x 3.6864MHz (=14.7456MHz), and the ECLK signal is 1.8432MHz or 3.6864MHz.

4. Bus Operation

   The microprocessor operates in expanded memory mode and executes firmware contained in memory, U715. The microprocessor uses a non-multiplexed address data bus, consisting of data lines D0 thru D7 and address lines A0 thru A15. In addition, the microprocessor has integrated chip-select logic so that external memories can be accessed without the need for external address decoder gates. These chip-select signals are provided by pins U705-PG5, PG6, and PG7.

   The SLIC (U710) provides an extra 32 I/O ports which can be accessed as byte-wide memory locations. These ports are used to generate additional control signals or to read more input signals. In addition, the SLIC also provides a memory-management function (MMU). Since the microprocessor only provides 16 address lines, it can only directly address 64K (= 2^{16}) of external memory. The SLIC contains logic to switch in 16K blocks of Flash memory, so that larger address space can be realized.

   When the controller board is functioning normally, the microprocessor's address and data lines should be toggling at CMOS logic levels. Specifically, the logic-high levels should be between 4.8 and 5.0V, and the logic-low levels should be between 0 and 0.2 V. No other intermediate levels should be observed, and the rise and fall times should be < 30 nsec. The low-order address lines (A0-A4) and the data lines (D0-D7) should be toggling at a high rate; e.g., you should set your oscilloscope sweep to 1 µsec/div or faster to observe individual pulses. High-speed CMOS transitions should also be observed on the microprocessor control lines such as R/W* (U705-B6), and the chip-select lines U705-PG7, PG6, and PG5. Another line of interest is the MODA line, pin U705-C5, which is also connected to U703 pin 1 and R727. While the CPU is running, this signal is an open-drain CMOS output which goes low whenever the µC begins a new instruction (an instruction typically requires 2-4 external bus cycles, or memory fetches). Since it is an open-drain output, however, the waveform rise assumes an exponential shape similar to an RC circuit.

   On the microprocessor (U705), the lines XIRQ (pin E8) and RESET (pin E5) should be high during normal operation. Whenever a data or address line becomes open or shorted to an adjacent line, a

common symptom is the RESET line goes low periodically, with the period being on the order of msec.

5. RAM

   The on-chip 1k static RAM from U705 provides some scratch-pad memory, with the bulk of it coming from the external 32K SRAM U714. External SRAM accesses are indicated by the CSGEN signal U714 pin 20 (which comes from U705-PG6) going low. Normally RAM is accessed less often than the Flash U715; i.e., the number of transitions per second on U715 chip select (pin 30) should be 5-15 times higher than those on U714 pin 20.

6. EEPROM

   The so-called radio codeplug storage is provided by U705's internal 512 byte EEPROM, with an additional 8K or 32K bytes of data provided by external EEPROM U713. There are three basic types of codeplug information: information on the trunked system(s) on which the radio is authorized to operate, information on the conventional system(s), which is either of the repeater or talk-around type on which the radio is authorized to operate, and information on the configuration and tuning of the radio itself. Note: tuning information is located in the internal memory of U705.

7. SB9600 Serial Interface

   The radio uses a proprietary multiprocessor serial protocol known as SB9600. This protocol allows the microprocessor in the system to interface to an external PC (for programming using RSS), a remote hand-held mic, or a vehicular adapter.

   From a hardware standpoint, this interface is comprised of the universal connector lines LH BUSY and LH DATA (P403 pins 9 and 11, respectively). The LH DATA signal is a bidirectional 0-5V RS-232 line that uses U705's integrated RS-232 asynchronous serial communications interface (SCI) peripheral, with the SCI TX line being U705-PD1 and the SCI RX line being U705-PD0. The SCI TX line is connected to the controller board signal LH DATA through Schottky diode CR702. This diode allows the SCI TX line to drive LH DATA active low only; when SCI TX is high, the diode does not conduct and LH DATA is pulled high by 10K resistor R743. The LH DATA line is connected to U705's SCI RX line through analog switch U709, which is normally closed unless the radio is in the Flash programming mode, as previously discussed. The LH DATA signal is routed to the controller connector J701 pin 26 via analog mux U711, which is normally configured to select signals X0, Y0, and Z0 by virtue of the common control signal MUX CNTL being a logic low.

   The LH BUSY signal, which is labelled BUSY on the controller schematic, is connected to two digital ports: U705 input PA1, and U710 output PL6. The BUSY signal is a bidirectional active-high signal that is normally pulled down by 10K resistor R739. It is routed to the controller connector J701 pin 22, via U711 pins 2 and 15.

   A typical usage of the SB9600 interface is using a PC running the RSS software package and the radio interface box (RIB) to program the radio's codeplug. When the PC sends a command or data to the radio, one should observe the SCI RX line (U705-PD0) toggling at a 9600 baud rate, and the BUSY line going high when data is actually being sent. After data transfers are completed, the BUSY line should idle low and the LH DATA line should idle high. The controller board also sends a power-up status message when it is first turned on, so one should be able to observe SB9600 data being sent from the radio within a few msec after power-up.

8. SPI Interface

   The microprocessor communicates to several ICs and modules through a dedicated on-chip serial peripheral-interface (SPI) port which consists of transmit data line MOSI (U705-PD3), receive data line MISO (U705-PD2), and clock line SCK (U705-PD4). In addition, each IC that can be accessed by the multiprocessor using the SPI has a select line associated with it. The programmable ICs or circuits and their associated select lines are:

   - the ASFIC (U701), with select line U705-PG3,
   - the transceiver board reference oscillator (U203), with select line U705-PG1,
   - the transceiver board synthesizer (U204), with select line U705-PG0,
   - the transceiver board IF IC (U3), with select line U710-PL4,
   - the transceiver board D/A with select line U710-PD5,
   - the LCD display board, with select line U710-PK6, and
   - the secure/data board, which has two independent select lines, U710-PK5 and U710-PK0.

   For all these SPI devices, the select lines are active-low; i.e., the select line goes low only when the associated device is being programmed. The first five ICs are listen-only; i.e., they cannot output data on the MISO line.

   The LCD keypad/display board uses the master out/slave in (MOSI) line to send data to the display driver IC, and the master in/slave out (MISO) line to send keypad data back to the controller multiprocessor. Note, however, that the keypad (or any other SPI device) can never initiate display data; the multiprocessor is at all times the SPI master device. Thus the MOSI line, and the MISO line are always in the master configuration. When a key is pressed, logic in the keypad board causes the KEY INT line

(J701 pin 9) to go low. The multiprocessor detects this transition using U710, and then sends a command to the display in order to read the keypad data.

The secure/data option board, which connects to connector jack J702, supports two slave SPI devices, which can each return data to the multiprocessor. The connector pins for these devices are J702 pins 21 and 23, and the interrupt lines (which performs the same function as the KEY INT line above) J702 pins 20 and 22. These lines connect to the SLIC IV (U710) at PK5, PK0, PH4, and PJ4, respectively.

9. Option Select Lines

The two option select lines OPT SEL 1 and OPT SEL 2, pins 1 and 5 of the universal connector, are used to identify the presence of external accessories and also to key up the radio with an external microphone. Table 1 (previously illustrated in the closed architecture controller section) shows the modes indicated by the various combinations of the signal states. Note that both signals have pullup resistors on the controller board (R702 and R717), so that if no external device is connected to these pins, they will be at a logic-high level and the radio will be in the normal mode; i.e., internal speaker and microphone will be used. Note also that RF power will always be routed to the internal antenna port unless a side connector is installed that activates the electro-mechanical switch inside the transceiver board which redirects power to the external antenna port. The microprocessor has no knowledge or control of which port transceiver energy is being directed. An external PTT (OPT SEL 1 =0, OPT SEL 2=0) will cause the external mic audio port to be activated, but the RF could be routed through either RF port.

10. LED Control

The bicolor LED on the top of the radio is activated by U710 output ports PK7 and PL7, in conjunction with the dual NPN transistor IC, U704. When either output is at logic high, the corresponding output pin of U704 (pin 6 for the green LED, pin 3 for the red) should be at approximately 4.3 volts. Note that it is possible to have both LED outputs on simultaneously, in which case the LED emits a yellow/ orange light.

11. Secure Board Interface

The radio can provide secure voice encryption using an optional secure board (with a number of possible encryption algorithms) connected to connector jack J702. A standard Motorola key-variable loader can be used to transfer key to the secure board. The keyloader connects the signals DVP WE, KID, and KEY/FAIL to the radio universal connector pins 7, 9, and 11, which correspond to controller connector jack, J701 pins 21, 22, and 26. In addition, the key-variable loader identifies itself by grounding universal connector pins 10 and 12, which correspond to controller connector jack, J701 pins 23 and 25. When the microprocessor detects these pins at a logic-low level, it then sets the control line labelled MUX CNTL for mux U711 to a logic one, which causes it to select the lines X1, Y1, and Z1. These are the DVP WE, KEY INSERT DATA, and KEY/FAIL lines from the secure board connector jack J702. The keyloader can then be used to transfer keys to the secure board.

B. Controller Board Circuit Operation

The circuits to be considered here are:

- the transmit audio path between the microphone and the transmit RF section,
- the transmit data path between the microprocessor and the RF section,
- the receive audio path between the receive RF section and the speaker,
- the receive data path between the receive RF section and the microprocessor, and
- the alert tone path between the microprocessor and the speaker.

The transmit and receive audio paths are disabled in the standby mode and selectively enabled by the microprocessor when the radio transmits or receives a signal. Also, there are minor differences in the functioning of both paths depending on whether an internal or external (accessory) microphone/speaker is being used. The radio constantly monitors the received data path for control-channel data in trunking operation or sub-audible data in conventional operation.

1. Transmit Audio Circuits

There are three major circuits in the transmit audio path. Some require enable lines and some are active devices that are always operating. When the operator presses the PTT while in trunked mode, the radio will request a channel from the control channel. When it receives a grant it will move to the specified voice channel and the microprocessor will enable the path between the microphone and the RF section. When the operator presses the PTT while in conventional mode, the radio will first monitor the channel for traffic (smart PTT) and if it is not busy the microprocessor will enable the path between the microphone and the RF section.

The microphone used in the radio front cover (internal mic) and remote microphone (external mic) are of the FET electric type and, thus, require a dc biasing voltage provided by R703 and R706, respectively. Note that there are two distinct microphone audio input paths (U701-A7 and U701-B8) for amplification; logic inside the ASF IC (U701) is used to select one of the signals.

a. Internal Mic Path

The internal microphone is located on the front cover of the radio and is connected to the controller board via J701-7. From here the signal is routed to R706 and R707. R706 is the dc biasing resistor and R707 provides input protection for the CMOS amplifier input. Filter capacitor C617 provides low-pass filtering to eliminate frequency components above 3kHz, and C713 serves as a dc block. The high-pass filter formed by C793 and R700 attenuates objectionable low-frequency audio components of speech.

b. External Mic Path

The external microphone signal enters the radio on universal connector pin 3 and is connected to the controller board via connector jack J701 pin 14. It is then routed to U701 through resistor R704 and capacitors C712, with dc bias provided by resistor R703.

c. PTT Sensing and Transmit Audio Processing

Depression of the internal PTT switch is detected via U710 port PH6, which has an internal pullup resistor. An external PTT is generated by grounding both the OPT SEL 1 and OPT SEL 2 lines on the universal connector (pins 1 and 5). These lines are read by U710 ports PJ5 and PJ6. When the internal PTT is sensed, the microprocessor will always configure the ASF IC for the internal mic audio path, and external PTT will result in the external mic audio path being selected. Inside the ASF IC, the mic audio is amplified, filtered to eliminate components outside the 300-3000Hz voice band, pre-emphasized, and then limited. The limited mic audio is then routed through a summer, which is used to add in PL or DPL sub-audio band modulation, and then to a splatter filter to eliminate high frequency spectral components generated by the limiter. After the splatter filter, the audio is routed to the two modulation attenuators, which are tuned in the factory or the field to set the proper amount of FM deviation. The TX audio emerges from the ASF IC at U701-H8, at which point it is dc coupled and applied through connector jack J704 pin 3 to the synthesizer (U204) pin 5.

d. HearClear (Compression) 900MHz Units Only

The HearClear IC provides proprietary circuitry to reduce audio noise and pops that can occur in a 2.5kHz deviation system (as in the 900 MHz RF band) when the radio is experiencing periodic signal fades that occur when, for example, the user is moving in a car. The overall TX audio path is the same as for the non HearClear TX audio except that the pre-amplified mic audio is looped through the compressor. More specifically, the ASF IC MIC audio output (U701-A6), which is nominally 80mVrms for an 8 mVrms mic input, is routed to U601-D3 via coupling cap C614. The input signal is compressed in a 2 to 1 ratio relative to an 80mVrms equal gain point. The output of the compressor is routed back to the ASF IC on pin U701-C7 through coupling capacitor C616. The ASF IC control line GCB4 (U701-A2), which connects to U601-D1, controls whether compression is enabled or disabled, and U601-C4 (which is generated by the ASF IC line U701-A3), controls whether the IC itself is enabled. The HearClear IC is enabled (logic high) at all times. The compressor/expander enable line is usually low (disabled) unless the radio is keyed up or receiving audio.

e. Secure Transmit Audio

The audio follows the normal transmit audio processing until it emerges from the ASF IC pre-emphasis out pin (U701-C8), which is fed to the secure board (J702 pin 7). The secure board contains circuitry to amplify, digitize, encrypt, and filter the audio. The encrypted signal is then fed back from J702 pin 14 to the ASF IC AUX TX input (U701-D7). The signal level at this pin should be about 1 Vpp. The signal is then routed through the AUX TX path (which bypasses the ASF IC splatter filter) and summed into the main modulation path. After the summer, it runs through the modulation attenuator and then to the VCO MOD port, the same as all other TX audio.

2. Transmit Data Circuits

There are four major types of transmit data: sub-audible data (PL/DPL/Connect Tone) that gets summed with voice, high-speed (3600 baud) data for trunking control channel communication, DTMF data for telephone communication in trunked and conventional systems, and MDC data for use in Motorola proprietary MDC systems. The deviation levels of the latter three types are tuned by a 5-bit digital attenuator inside the ASF IC. For each data type and each bandsplit, there is a distinct set of tuning values that are programmed into the ASF IC before the data is generated and transmitted.

a. Sub-audible Data (PL/DPL)

Sub-audible data is composed of low-frequency PL and DPL waveforms for conventional operation and connect tones for trunked voice channel operation. (The trunking connect tone is simply a PL sine wave at a higher deviation level than PL in a conventional system.)

Although it is referred to as “sub-audible data,” the actual frequency spectrum of these waveforms may be as high as 250Hz, which is audible to the human ear. However, the radio receiver filters out any audio below 300Hz, so these tones are never heard in the actual system.

Only one type of sub-audible data can be generated by U701 at any one time. The process is as follows: using the SPI, the microprocessor programs the ASF IC (U701) to set up the proper low-speed data deviation and select the PL or DPL filters. The microprocessor then generates a square wave from U705-PA6 which strobes the ASF IC PL/DPL encode input U701-C3 at twelve times the desired data rate. (For example, for a PL frequency of 103Hz, the frequency of the square wave at U701-C3 would be 1236Hz.) This drives a tone generator inside U701, which generates a staircase approximation to a PL sine wave or DPL data pattern. This internal waveform is then low-pass filtered and summed with voice or data. The resulting summed waveform then appears on U701-H8 (VCO MOD), where it is sent to the transceiver board as previously described for transmit audio.

b. High-Speed Data

High-speed data refers to the 3600 baud data waveforms (ISWs and OSWs) used in a trunking system for high-speed communication between the radio and the central controller. To generate an ISW, the microprocessor first programs the ASF IC (U701) to the proper filter and gain settings. It then begins strobing U701-G1 (Trunking Clock In) with a square wave (from U705-PA5) at the same baud rate as the data. The output waveform from U701’s 5-3-2 State Encoder is then fed to the post-limiter summer block and then the splatter filter. From that point it is routed through the mod attenuators and then out of the ASF IC to the transceiver board via the VCO MOD connector jack, J704 pin 3.

c. DTMF Data

DTMF data is a dual-tone waveform used during phone interconnect operation. There are seven frequencies, with four in the low group (697-941Hz) and three in the high-group (1209-1477Hz). The high-group tone is generated by U705-PA5 strobing U701-G1 at six times the tone frequency for tones less than 1440Hz, or twice the frequency for tones greater than 1440Hz. The low-group tone is generated by U705-PA4 strobing U701-G2 (DTMF CLOCK) at six times the tone frequency. Inside U701 the low-group and high-group tones are summed (with the amplitude of the high group tone being approximately 2dB greater than that of the low-group tone) and then pre-emphasized before being routed to the summer and splatter filter. The DTMF waveform then follows the same path as was described for high-speed data.

d. MDC Data

The MDC signal follows exactly the same path as the DTMF high-group tone. MDC data utilizes MSK modulation, in which a logic zero is represented by one cycle of a 1200Hz sine wave, and a logic one by 1.5 cycles of an 1800Hz sine wave. To generate the data, the microprocessor first programs the ASF IC (U701) to the proper filter and gain settings. It then begins strobing U701-G1 (Trunking Clock In) with a square wave (from U705-PA5) at the same baud rate as the data. The output waveform from U701 is fed to the post-limiter summer block and then the splatter filter. From that point it is routed through the mod attenuators and then out of the ASF IC to the transceiver board via the VCO MOD line, connector jack J704 pin 3.

3. Receive Audio Circuits

There are three major circuits in the receive audio path. These are the ASF IC (U701), the HearClear IC (U601), and the audio PA (U702). The ASF IC is an SPI-programmable device, while the other two ICs have direct control lines.

The radio’s RF circuits are constantly producing an output at the discriminator. Whenever the radio is in trunked standby mode, it is processing data from the control channel. While in conventional standby mode, it is always monitoring the squelch line and/or or sub-audible data. The raw discriminator from the transceiver board enters the controller board at connector jack J704 pin 10. In addition to the raw discriminator signal (DISC), the transceiver board’s IF IC also provides a pre-filtered version of the discriminator signal that is dedicated to the ASF IC squelch-detect circuitry. This signal, which is labelled SQ IN, enters the controller board at connector jack J704 pin 12, and is routed to the ASF IC on U701-H7. When the microprocessor is satisfied that it has received the proper data or signal type for unsquelching, it sets up the receive audio path and sends data to U701 to do the same within.

a. HearClear (Noise Muting)

For the 900MHz Hear Clear controllers, the raw discriminator (which contains both audio and sub-audible data) is routed to U601-E4, the input to the flutter fighter circuit inside U601. The purpose of this section is to eliminate any

noise bursts in the recovered audio due primarily to multi-path fades. The IC monitors the noise content of the discriminator as well as the received signal strength indicator (RSSI) line from the transceiver board. The IC then determines if the discriminator needs noise reduction (attenuation) and processes the signal accordingly. The output of the flutter fighter is U701-F4. The flutter fighter circuit is controlled by U601-E3, which is at a logic high when enabled. If this control line is low, the circuit will still pass audio but it will behave like a linear 0 dB gain stage without any noise reduction function.

b. U701 Audio Processing and Digital Volume Control

For a controller equipped with HearClear (U601), the signal next enters the ASF IC (U701-H6) for further processing. (For a non-Hear Clear controller, the signal enters via the PL IN line, U701-J7.) Inside the IC, the signal first passes through a low-pass filter to remove any frequency components above 3000Hz and then a high-pass filter to strip off any sub-audible data below 300Hz. Next, the recovered audio passes through a de-emphasis filter to reduce the effects of FM noise. Finally, the IC amplifies the audio and passes it through the 8-bit programmable attenuator whose level is set depending on the value of the volume control, or in the case of HearClear, it is first routed to the expander U601-C1 via pins U701-H5 and U701-J5 and then through the 8-bit attenuator. The microprocessor (U705) programs the value of the 8-bit attenuator in accordance with the voltage sensed on the volume potentiometer, which is connected to U705-PE2. This pin is one of the eight channels of U705's 8-bit A/D converter. After passing through the 8-bit digital attenuator, the audio goes to a buffer amplifier and then exits at U701-J4, where it is routed to the Audio PA, U702.

c. HearClear (Expansion)

In the HearClear mode, the de-emphasized audio is routed through the HearClear expander and back to the ASF IC. Audio enters the expander on pin U601-C1 and exits on U601-A2. The expander input signal is expanded in a 1 to 2 ratio (which cancels the 2 to 1 compression on transmit) relative to a 200mVrms equal gain point. Control line U701-D1 controls whether expansion is enabled or disabled. If this signal is at a logic-low level then the expander still passes audio but behaves like a linear gain stage with +3 dB of gain.

d. Differential Speaker Audio Amplification

The final stage in the receive path is the audio amplifiers that drive either the internal or external speakers. Each speaker is driven using a dual- amplifier arrangement. Since one amplifier can be shared as common between the two speakers, only three total amplifiers are needed inside the audio PA IC, U702. Audio is coupled into the amplifiers on U702-C6.

There are two enable lines controlling the three audio amplifiers of U702. The external speaker select line, which is used to control the phase of the internal or external amplifier, comes from U701-B4, and the audio PA enable line (which is used to enable all three amplifiers) comes from U710-PK4. The audio PA enable line is active-high, while the external speaker select is active-low, i.e., the external speaker is selected if this control line is at a logic low; and the internal speaker otherwise. The microprocessor determines that audio should be routed to the external or internal speaker by reading the option select lines 1 and 2, which are pins 1 and 5 of the universal connector. If the microprocessor reads these OPT SEL 1 to be 0 and OPT SEL 2 to be 1, and the radio is in receive audio mode, the audio will be directed to the external speaker lines (pins 2 and 6 of the universal connector) with the audio level being controlled by the radio volume pot. If the microprocessor senses that there is a vehicular adapter connected to the radio (which is identified by having a diode from OPT SEL 2 to OPT SEL 1, with the anode at OPT SEL 2), and the radio is in receive audio mode, the audio will be directed to the external speaker lines (pins 2 and 6 of the universal connector) with the audio set to a fixed level, independent of the radio volume pot. When the receive path is to be enabled, the microprocessor sends data to U710 to put a high on U710-PK4 which turns on all three amplifiers. If the internal speaker amplifier is selected, then its output is 180 degrees out of phase with the output of the common amplifier. The result at the internal speaker is a signal twice as large as either amplifier's output, while the external amplifier is in phase with the common amplifier; the result at the external speaker is no signal. The reverse is true if the external speaker is selected. The nominal voltage for rated audio is 3.74Vrms, and the nominal audio input to U702 is 88.7mVrms when rated audio output is obtained.

e. Secure Receive Audio

Discriminator audio is routed to the secure board via connector jack J702 pin 10. On the

secure board it is decrypted and converted back to analog format, and then fed back to the ASF IC from the AUX RX line (J702 pin 9). It is then routed to the ASF IC pin U701-J6; from then on it traverses a path identical to conventional receive audio

4. Receive Data Circuits

   The ASF IC (U701) decodes all receive data, which includes PL, DPL, low-speed trunking, MDC, and high-speed trunking data. The “decode” process for each data type typically involves low-pass or bandpass filtering, signal amplification, and then routing the signal to a comparator, which outputs a logic zero or one signal. The discriminator output from the transceiver board is routed to U701-J7 through coupling capacitor C709. Inside U701, the data is filtered according to the data type (HS data or LS data), then hard-limited to a 0–5V digital level. The high-speed limited data output (MDC and trunking high-speed) appears at U701-G4, where it connects to U705-PA0. The low-speed limited data output (PL, DPL and trunking low-speed) appears at U701-A4, where it connects to U710-PK7. If, for example, the radio is receiving 192.8Hz PL, the discriminator should contain a 192.8Hz sine wave at about 53mVrms, and the limited PL output should be a 192.8 Hz square wave. While the radio is decoding PL, DPL, or low-speed trunking data, the microprocessor also outputs a sampling waveform on U705-PA6, which is routed to U701-C3. (This is the same line used to generate TX PL or DPL data.) This sampling waveform is a square wave between 1000 and 2000Hz.

5. Alert Tone Circuits

   When the microprocessor needs to give the operator feedback (for a good key press or for a bad key press) or radio status (trunked system busy, low battery condition, phone call, circuit failures), it sends an alert tone to the speaker. It does so by sending data to U701, which sets up the audio path to the speaker for alert tones. The alert tone itself can be generated in one of two ways: internally by the ASF IC, or externally using the microcontroller and the ASF IC. The allowable internal alert tones are 300, 900, and 1800Hz. For external alert tones, the microcontroller can generate any tone within the 100-3000Hz audio band. This is accomplished by the microprocessor toggling the output line U705-PA4, which is also the same line used to generate low-group DTMF data. Inside the ASF IC, this signal is routed to the external input of the alert tone generator. The output of the generator is summed into the audio chain just after the RX audio de-emphasis block. Inside U701, the tone is amplified and filtered, then passed through the 8-bit digital volume attenuator. (Note that the expander is bypassed even if U601 is present.) The tone exits at U701-J4, then is routed to the audio PA the same as receive audio.

VII. UNIVERSAL CONNECTOR (See Tables 2 and 3)

The universal connector (radio side connector) consists of 13 pins, many of which serve multiple functions. The various pins will be discussed by function.

Pins 1 and 5 are the option selection lines, OPT SEL 1 and OPT SEL 2, respectively. The state of these pins informs the radio microcontroller of the type of accessory attached, and the operating mode of the accessory. For example, an external speaker microphone will select external speaker by pulling OPT SEL 1 low, and will indicate PTT by pulling both OPT SEL 1 and OPT SEL 2 low. Refer to Table 2 for details.

Pin 2, the EXT SPKR line, and pin 6, the SPKR COMM line, provide the two signals required for the differentially driven external speaker.

Pin 3, the EXT MIC line, is used for external microphone audio.

Pin 4, the OPT B+/BOOT PGM SEL pin, serves two functions. This pin is normally used to provide current limited SW B+ to an external accessory. For special purposes, most commonly reprogramming the Flash memory in the radio, this pin serves another function. This pin is also able to put the microprocessor in a special “bootstrap” mode. This allows software to be loaded into the processor to reprogram the Flash memory device.

Pin 7, the AUX TX/RSSI/RX OUT/DVP WE/RTS pin, serves many functions depending on the radio mode of operation. This pin is multiplexed by the MUX (U711), the ASF IC (U702), and the SLIC, U710. This pin serves as an analog input for AUX TX when used for modulation balance adjustments when programmed by the RSS. It serves as an analog output of RSSI information when tuning front-end filters in UHF and VHF radios when programmed by the RSS. It serves as an analog output of buffered discriminator signal when tuning discriminator level with the RSS (secure equipped radios). It serves as a digital input for the key-variable loader (KVL) WE signal when the key-variable loader is attached.

Pin 8 is controller board ground. This is an independent ground path from the RF ground, which is also on the universal connector.

Pin 9, the LH BUSY/KID/DATA IN line, serves several functions. During normal radio operation, this pin is used for the BUSY signal for SB9600 communications. When a key-variable loader is attached, this pin carries the key insert data (KID) signal.

Pin 10, the Vpp/CTS pin, also serves several functions. When reprogramming the Flash memory device, this pin carries the programming voltage, Vpp. The pin is also used to identify that a key-variable loader is attached. The KVL cable will ground this pin.

Pin 11, the BOOT PGM RX/TX DATA pin, is used for receive data during bootstrap programming, typically when reprogramming the Flash. Unlike normal SB9600 communications, bootstrap mode requires separate receive and transmit data paths.

Pin 12, MODE CNTRL, is used to identify that a "special" device is connected. Typically this will be the key-variable loader. Typically, the microcontroller will reprogram MUX CNTL high when this pin is low. The key-variable loader cable also grounds this pin.

Pin 13, LH DATA/ (KEY/FAIL), serves several functions as well. During normal radio operations, this pin is used as the bi-directional SB9600 data pin. When the key-variable loader is attached, this pin carries the bi-directional KEY/FAIL signal from the KVL. When the radio is in bootstrap mode, typically during Flash programming, this pin is used for transmit data. Unlike normal SB9600 communications, bootstrap mode requires separate receive and transmit data paths.

Table 2. Option Select Definition

MODE#	MODE	OPT SEL 1	OPT SEL 2	COMMENT
00	External PTT	0	0	
01	External Audio	0	1	External Speaker
10	Mandown	1	0	
11	Normal Operation	1	1	
A	MTVA			Fixed Audio Output Level
B	"Smart" SB9600 Accessory			Identifies SB9600 Accy.
C	External RF Modem/FAX			Enables AUX TX and Discriminator Audio Output

Table 3. Universal Connector Mode

OPTION B+	MODE CONTROL	MODE
NC or Load	No Connection	Normal
NC or Load	Ground	Special
>12 Volts	No Connection	Bootstrap Program

TROUBLESHOOTING

I. INTRODUCTION

Servicing the HT 1000, MT 2000, MTS 2000, and MTX series portable radios requires the localization of the malfunctioning circuit before the defective component can be isolated and replaced. Since localizing and isolating a defective component constitutes the most time consuming part of troubleshooting, a thorough understanding of the circuits involved will aid the technician in performing efficient servicing. The technician must know how one function affects another; must be familiar with the overall operation of the radio and the procedures necessary to place it back in operation in the shortest possible time.

The radio functional block diagrams, schematic diagrams, and troubleshooting charts provide valuable information for troubleshooting purposes. The functional diagrams provide signal flow information in a simplified format, while the schematic diagrams provide the detailed circuitry and the biasing voltages required for isolating malfunctioning components. By using the diagrams, troubleshooting charts, and deductive processes, the suspected circuit may be readily found.

To determine if analyzation of the radio is required, perform checks such as 20dB quieting, 12dB SINAD, noise and PL squelch sensitivity, for the receiver; and current drain for the transmitter. These should give the technician a general indication of where the problem is located.

After the general problem area of the radio has been identified, careful use of a dc voltmeter, rf millivoltmeter, and an oscilloscope should isolate the problem to an individual component.

II. TROUBLESHOOTING PROCEDURE

Each time that the radio is turned on, a microcomputer self-test occurs. A 1600Hz alert tone is generated for approximately 500 milliseconds to indicate that the microcomputer is functioning properly. If the alert tone is not heard (and the alert tones have not been disabled via the Radio Service Software), there is a problem with the radio.

Following the microcomputer self-test, a synthesizer self-test occurs. A continuous 1600Hz alert tone is generated if the synthesizer test is **not** successful. If this condition occurs (continuous alert tone) refer to the VCO/synthesizer troubleshooting chart.

When a radio performs unsatisfactorily, the following procedures should help localize the fault.

A. Check Batteries

The first step in localizing a problem is to check the battery voltage under load. With the transmitter turned on (keyed), check the battery voltage. A convenient way to do this is to remove the front cover and monitor the B+ line with a voltmeter (with respect to ground). The measured load voltage should not be less than seven volts. Even though the transmitter may operate at a lower voltage, operation would be marginal and for only a short period of time. Low-voltage transmit operation is indicated by the flashing LED on top of the radio. If the measured voltage is zero volts, check the battery. The recommended procedure is to replace, or recharge, the battery if the voltage is below seven volts under load.

B. Alignment

Strict adherence to the published procedures is a prerequisite to accurate alignment and proper evaluation of the performance of the radio. The selection of test equipment is critical. The use of equipment other than that recommended should be cleared through your Motorola Area Representative to ensure that it is of equivalent quality.

The service technician must observe good servicing techniques. The use of interconnecting cables that are too long, poorly positioned (dressed), or improperly terminated will result in erratic meter readings. As a result, it will not be possible to tune the radio to the desired specifications.

Use the recommended test equipment setup and proper connections for alignment and adjustments. Refer to the detailed procedures supplied in the applicable service manual.

C. Check Overall Transmitter Operation

If the battery voltage is sufficient, check the overall performance of the transmitter. A good overall check of the transmitter is the rf power output measurement. This check indicates the proper operation of the transmitter amplifier stages. A properly tuned and operating transmitter will produce the rated rf output into a 50-ohm load with a dc input of 7.5 volts (refer to "Transmitter Alignment Procedure," located in the service manual, for specific rf output). If the power is less than rated rf output, refer to the applicable transmitter troubleshooting chart.

D. Check Overall Receiver Operation

1. 20dB Quieting Sensitivity Test

   A good overall check of receiver operation is the 20dB quieting sensitivity measurement. This check will indicate that the receiver has sufficient gain and that all of the included circuitry is working properly. The quieting signal is that rf signal input necessary to reduce the audio output at the speaker by 20dB. This measurement should be made with no modulation. It will be necessary to hold the monitor button during this test, or the radio's squelch circuitry will remove the noise from the speaker.

   Make the actual measurement (using an ac voltmeter) by setting the noise voltage across the test box speaker load (with no rf signal received at the antenna) to one-half (1/2) of the rated audio power output (1.85Vrms). Sufficient carrier signal from a generator is then introduced via the antenna port to reduce the noise output voltage to one-tenth (1/10) of the previous reading. If all of the circuitry is operating correctly, this reading should be 0.5µV or less. If the radio does not meet this specification, try to retune the receiver using the procedure indicated in the service manual. If this does not solve the problem, refer to the receiver troubleshooting chart.

2. 12dB SINAD

   This procedure is a standard method for evaluating the performance of an FM receiver, since it provides a check of the rf, i-f, and audio stages. The method consists of finding the lowest modulated signal necessary to produce 50% of the radio's rated audio output with a 12dB or better ratio of signal + noise + distortion / noise + distortion. This is termed "usable sensitivity."

   To perform this measurement, connect the leads from a SINAD meter to the audio output of the test box. Set the Motorola service monitor or rf signal generator to output a 1-millivolt signal. Modulate the rf signal with a 1kHz tone at 3kHz deviation (VHF, UHF, 800MHz) 1.5kHz deviation for 900MHz. Introduce the signal to the radio at the exact channel frequency through the antenna port. Set the volume control for rated audio output (3.74Vrms). Decrease the rf signal level until the SINAD meter reads 12dB. The signal generator output (12dB SINAD measurement) should be less than 0.35µV. If the radio does not meet this specification, try to retune the receiver using the procedure indicated in the service manual. If this does not solve the problem, refer to the receiver troubleshooting chart.

III. VOLTAGE MEASUREMENT AND SIGNAL TRACING

To aid in troubleshooting, ac and dc voltage readings are provided (in red) on the transceiver schematic diagram in the service manual. When making these voltage checks, pay particular attention to any notes that may accompany the voltage reading of a particular stage.

If receiver sensitivity is high or if the rf power output is lower than normal for a fully tuned transceiver, the dc voltages on the printed circuit board should be checked. These voltages should be referenced to ground.

CAUTION

When checking a transistor or module, either in or out of the circuit, do not use an ohmmeter having more than 1.5 volts dc appearing across the test leads or an ohms scale of less than x 100.

It is recommended not to replace a transistor or module before a thorough check is made. Read the voltages around the suspected stage. If these voltages are not reasonably close to those specified, the associated components should be checked.

A low impedance meter should not be used for measurement. If all dc voltages are correct, the signal should be traced through the circuit to show any possibility of breaks in the signal path.

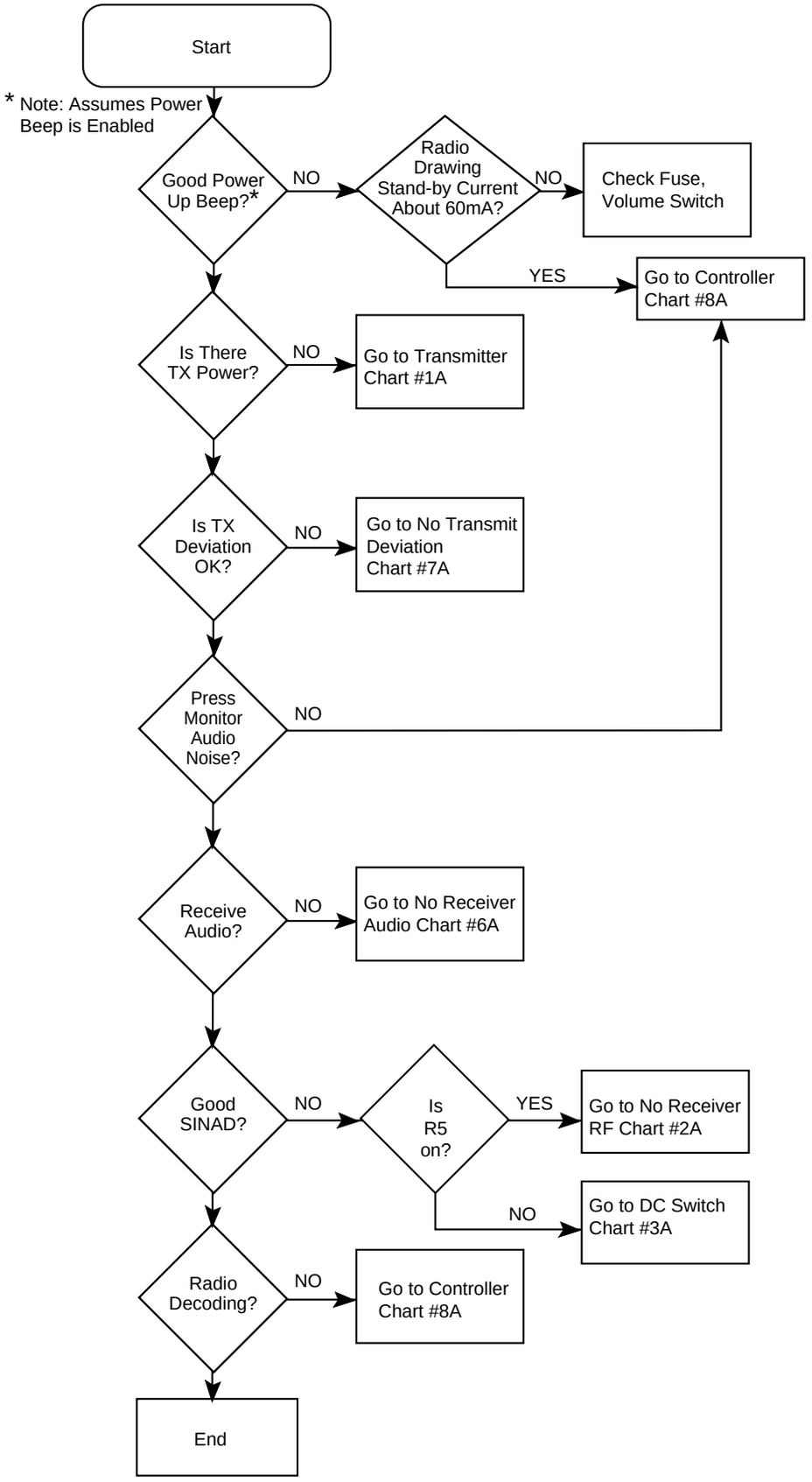
CAUTION

The microcomputer is a static sensitive device contained on the controller flex assembly. DO NOT attempt to troubleshoot or disassemble the microcomputer/controller flex assembly without first referring to the "Safe Handling of CMOS Devices" paragraph in the **MAINTENANCE** section of the manual.

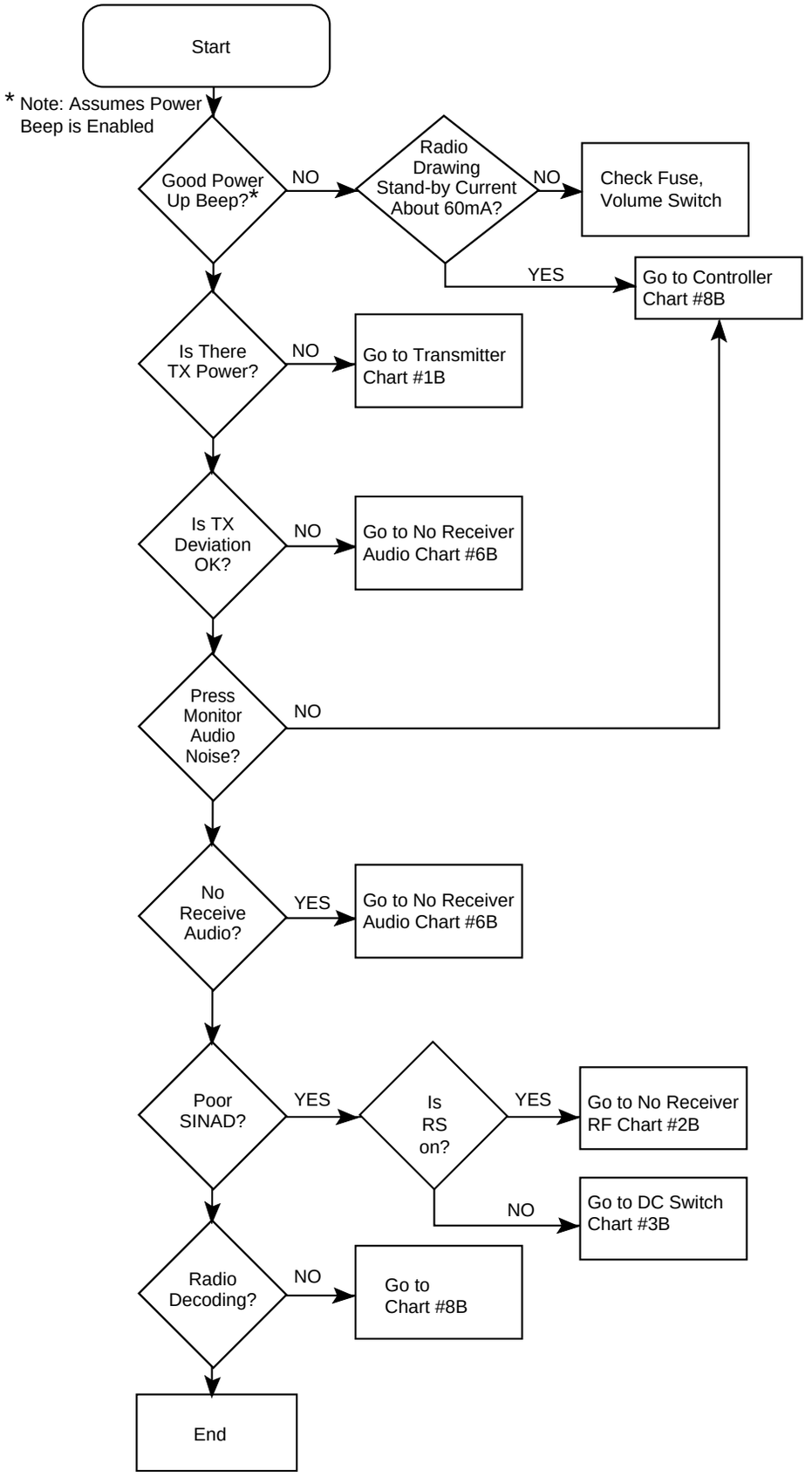
IV. TROUBLESHOOTING CHARTS

The troubleshooting charts on the following pages will help isolate troubles in the different sections of the radio. Start at the top of the appropriate chart and make the checks as indicated. Most usual malfunctions will respond to the systematic approach to troubleshooting. Also, a flowchart is provided to aid in choosing the proper troubleshooting chart.

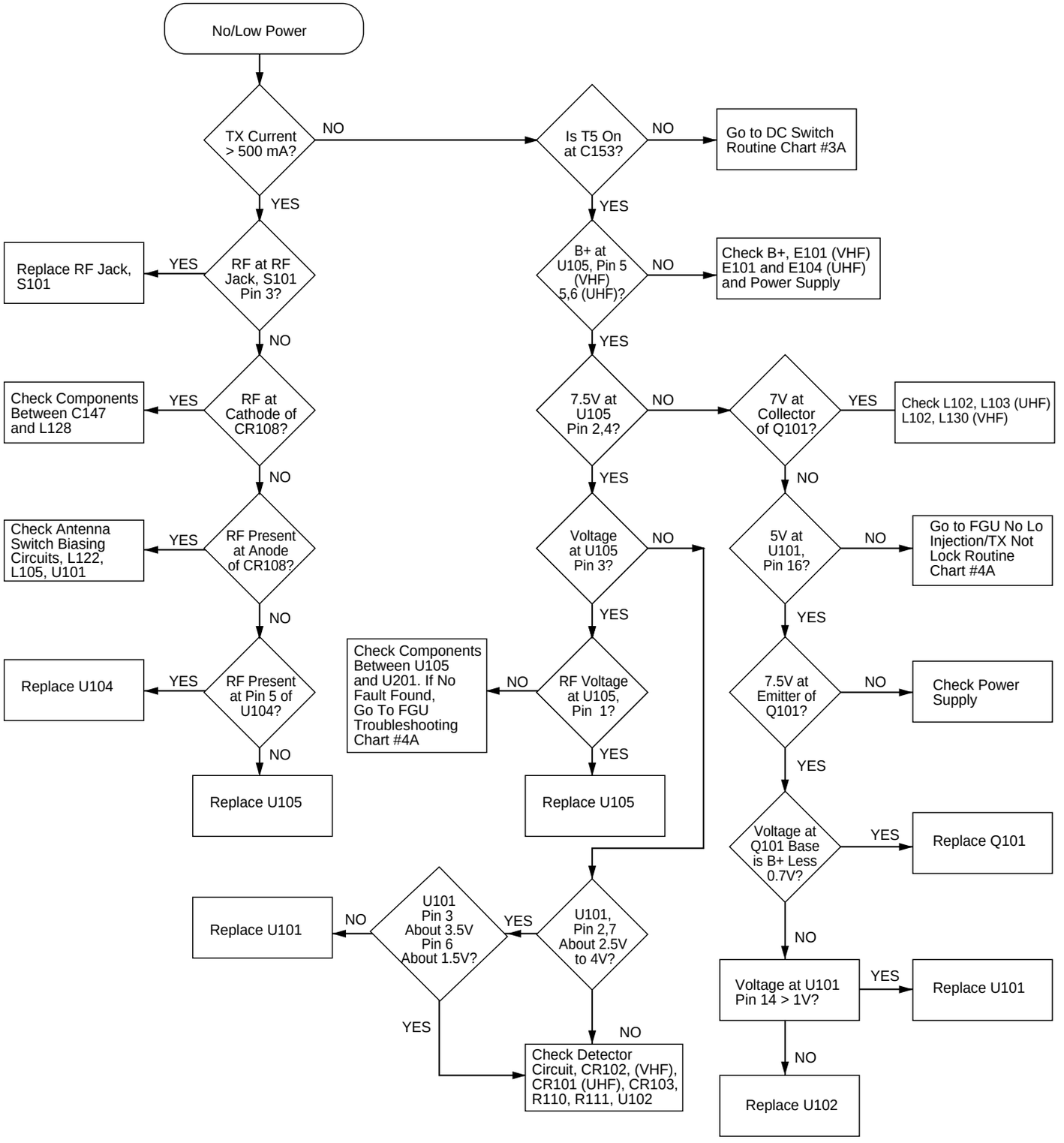
TROUBLESHOOTING FLOW CHART
(VHF/UHF Transceiver/Closed Architecture Controller)



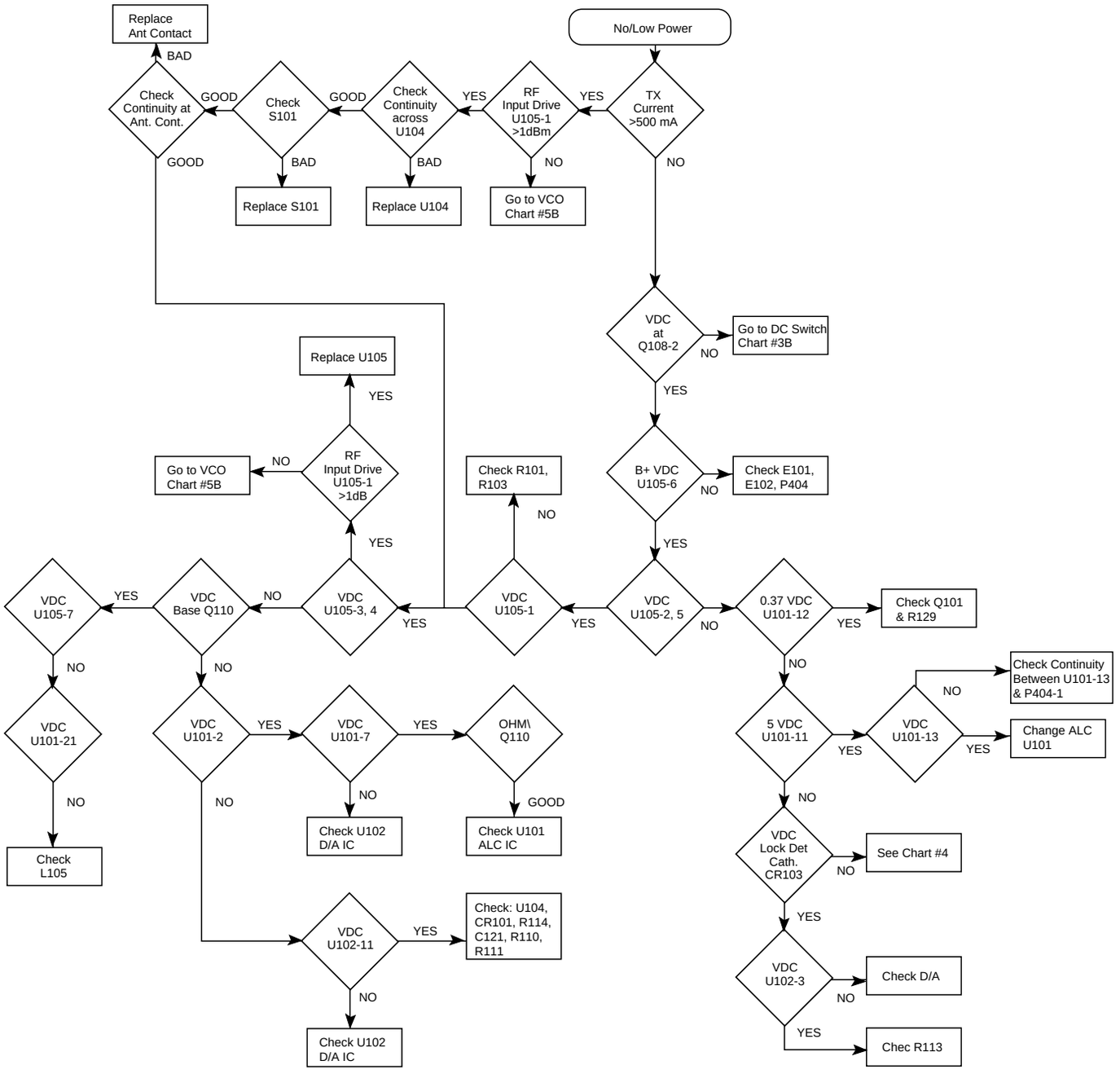
TROUBLESHOOTING FLOW CHART
(800/900MHz Transceiver/Open Architecture Controller)



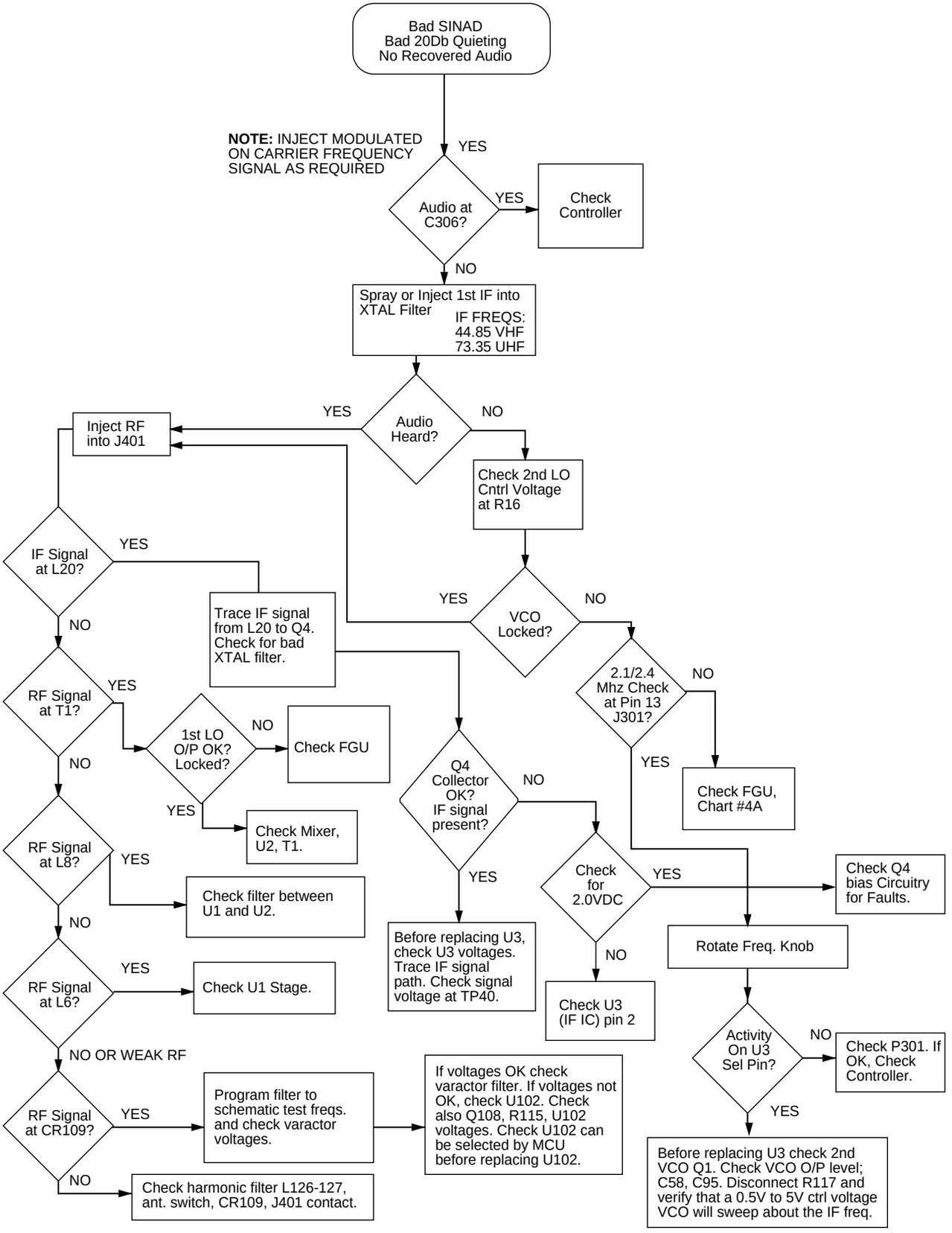
TROUBLESHOOTING FLOW CHART #1A
(VHF/UHF Transmitter RF)



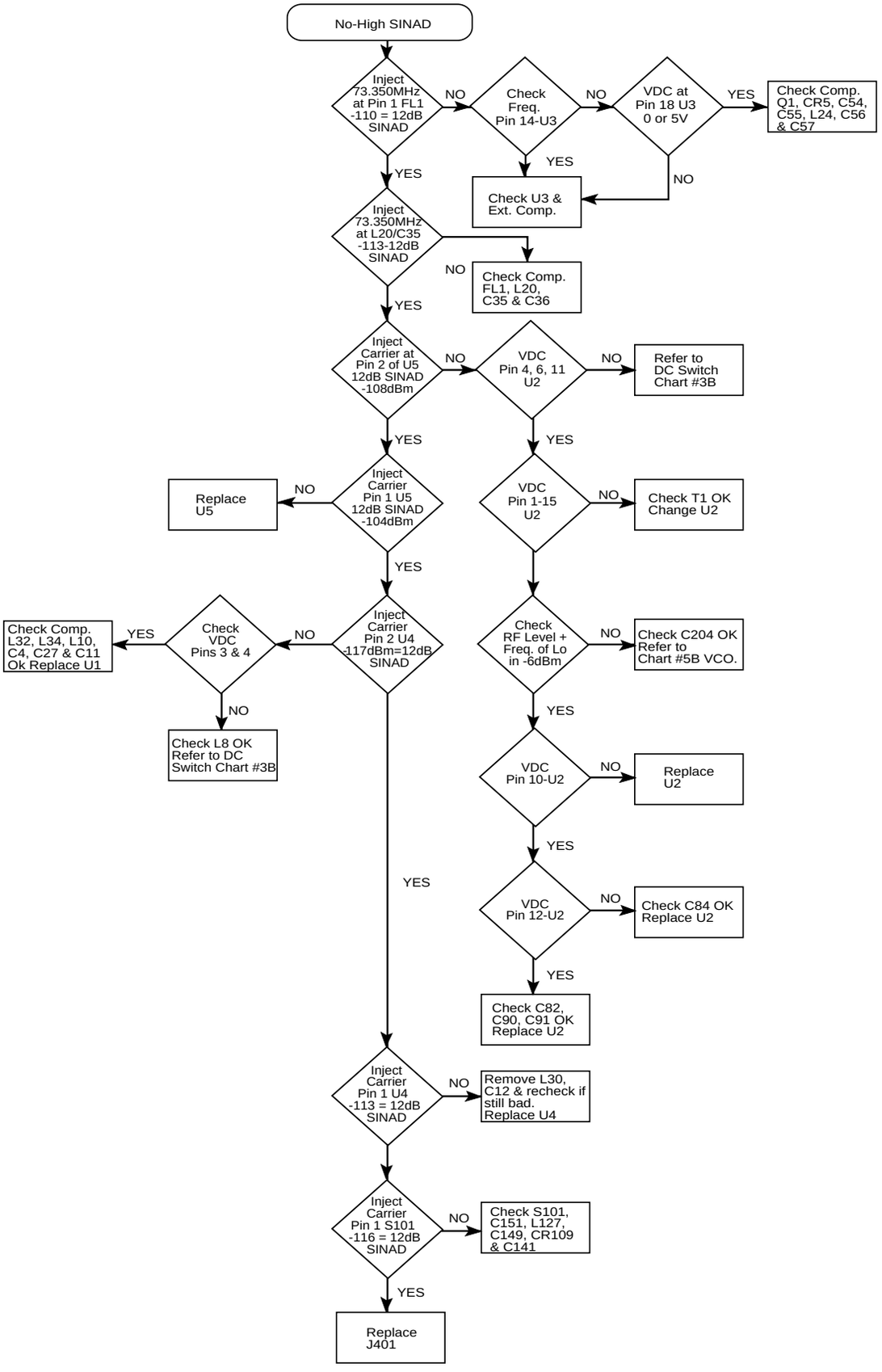
TROUBLESHOOTING FLOW CHART #1B
(800/900MHz Transmitter RF)



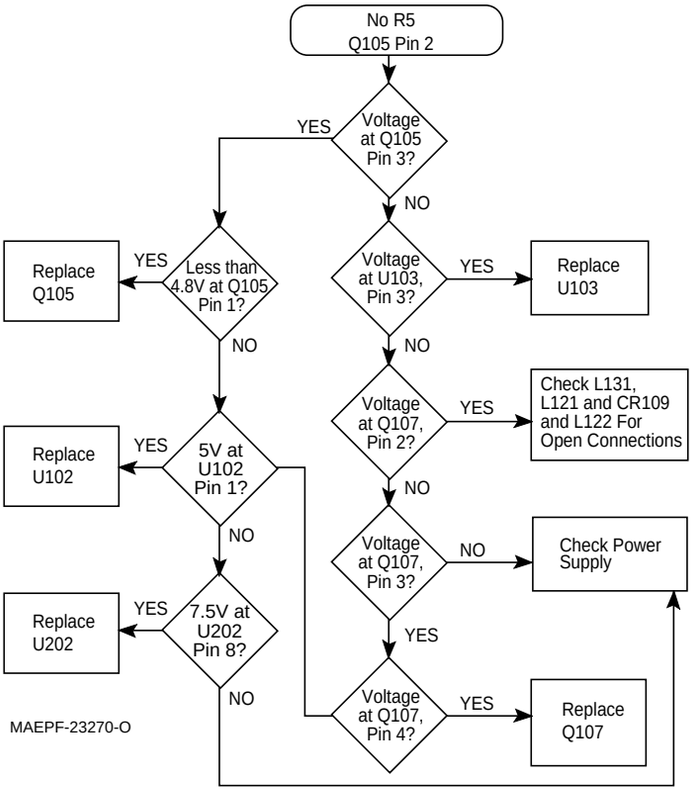
TROUBLESHOOTING FLOW CHART #2A
(VHF/UHF Receiver RF)

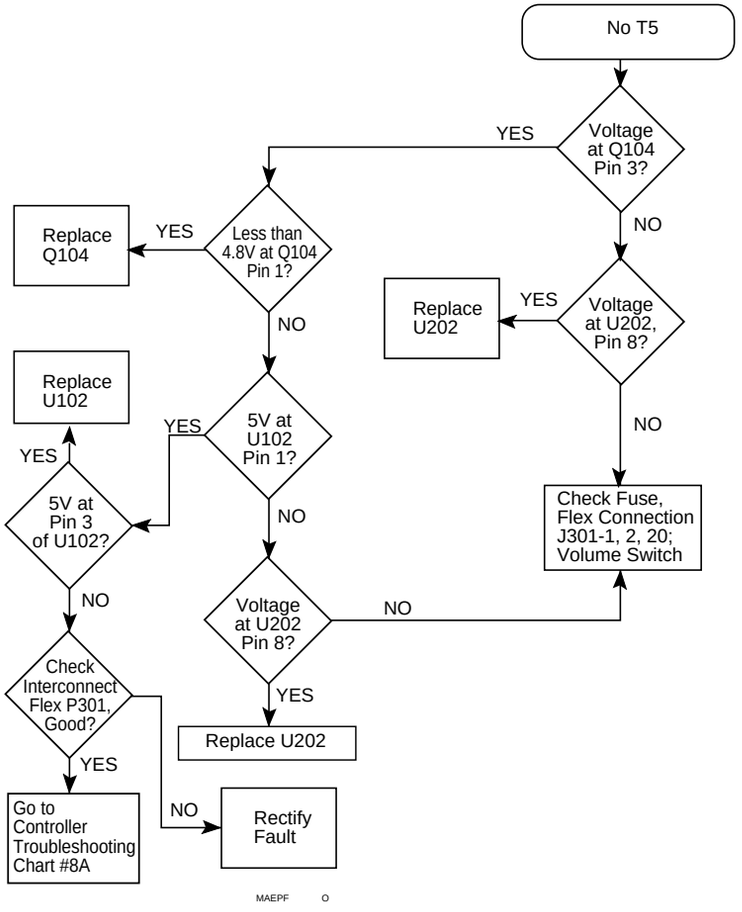


TROUBLESHOOTING FLOW CHART #2B
(800/900MHz Receiver RF)

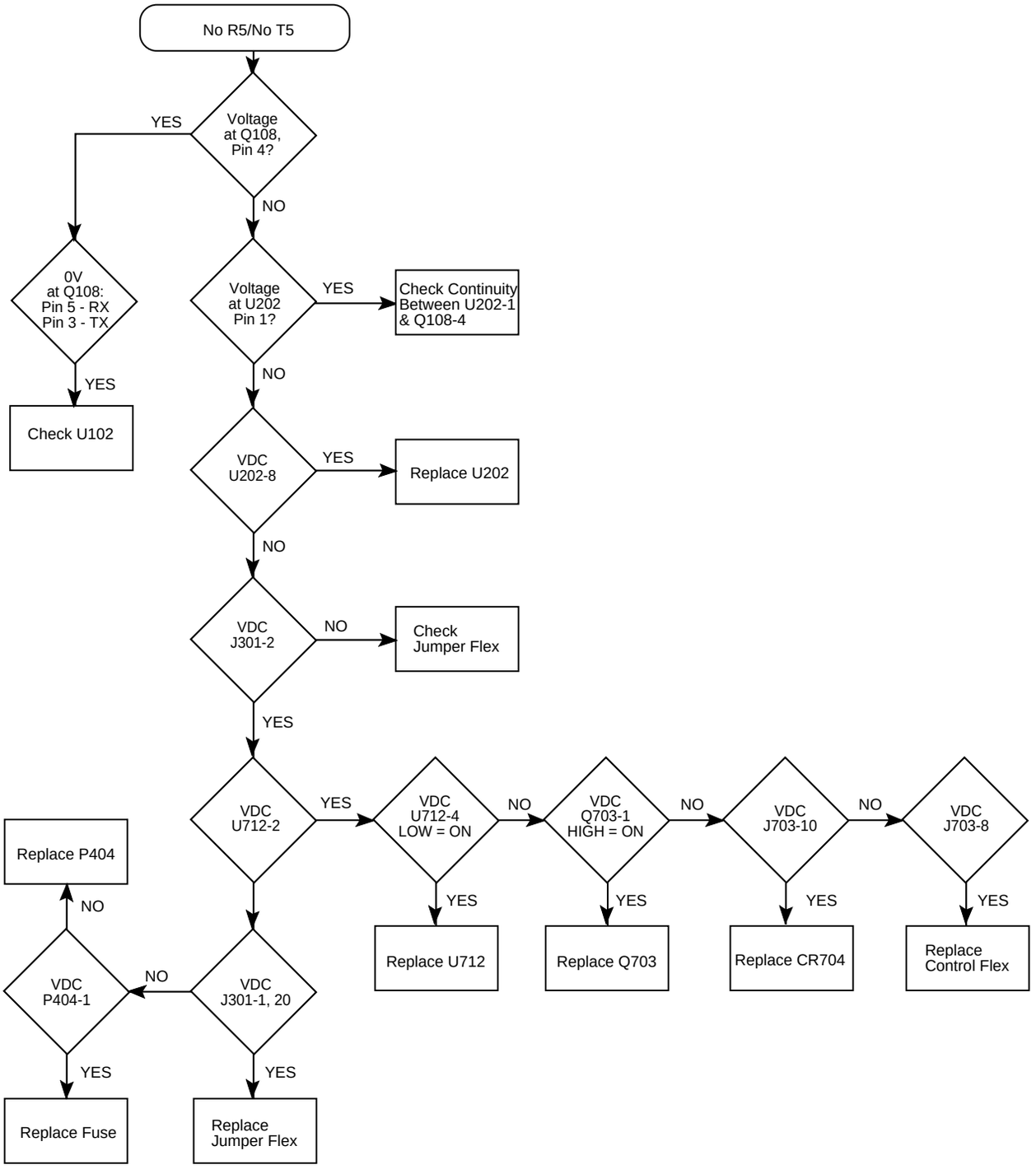


TROUBLESHOOTING FLOW CHART #3A
(VHF/UHF DC Switch)

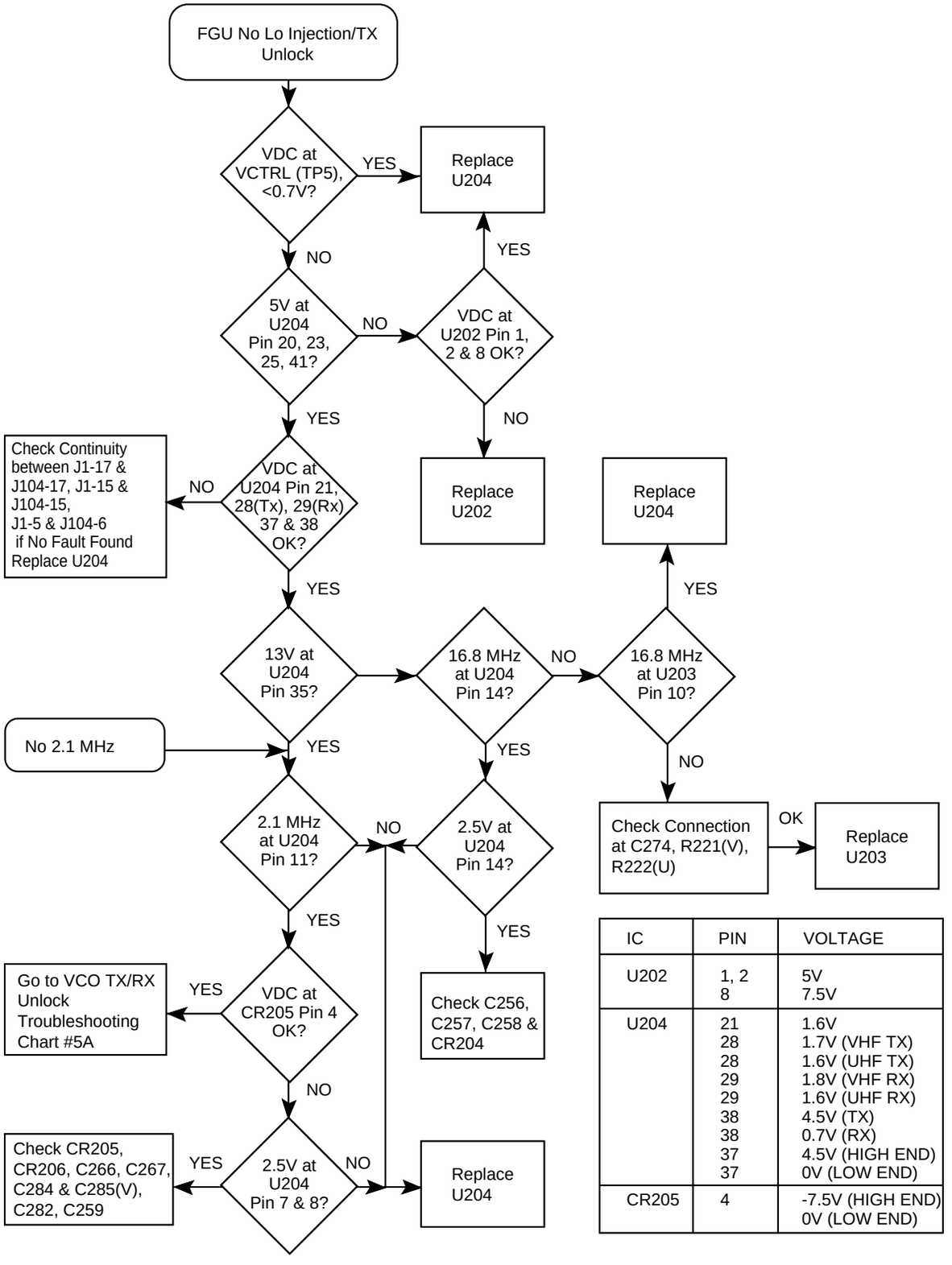




TROUBLESHOOTING FLOW CHART #3B
(800/900MHz DC Switch)

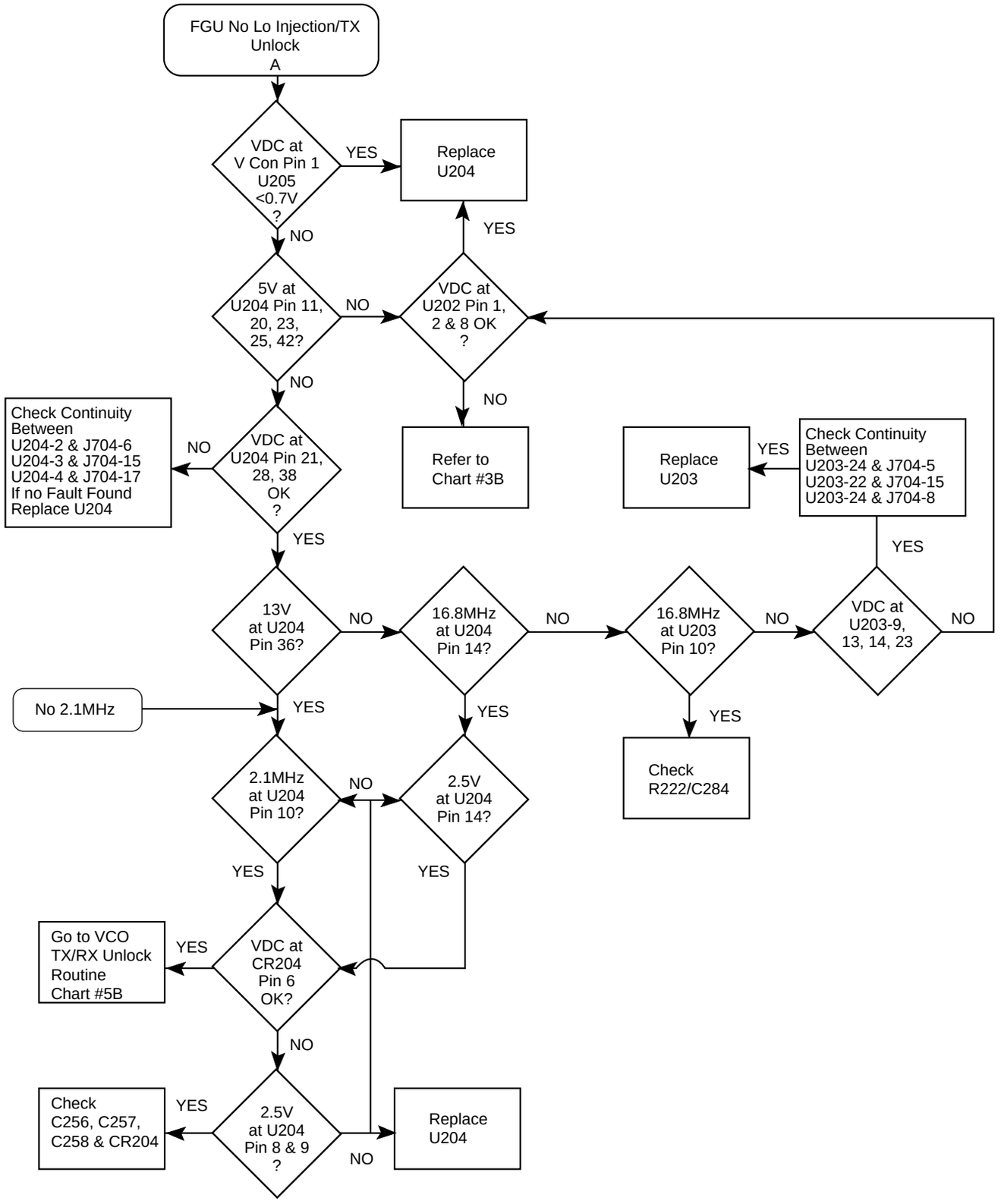


TROUBLESHOOTING FLOW CHART #4A
(VHF/UHF Frequency Generation Unit - FGU)

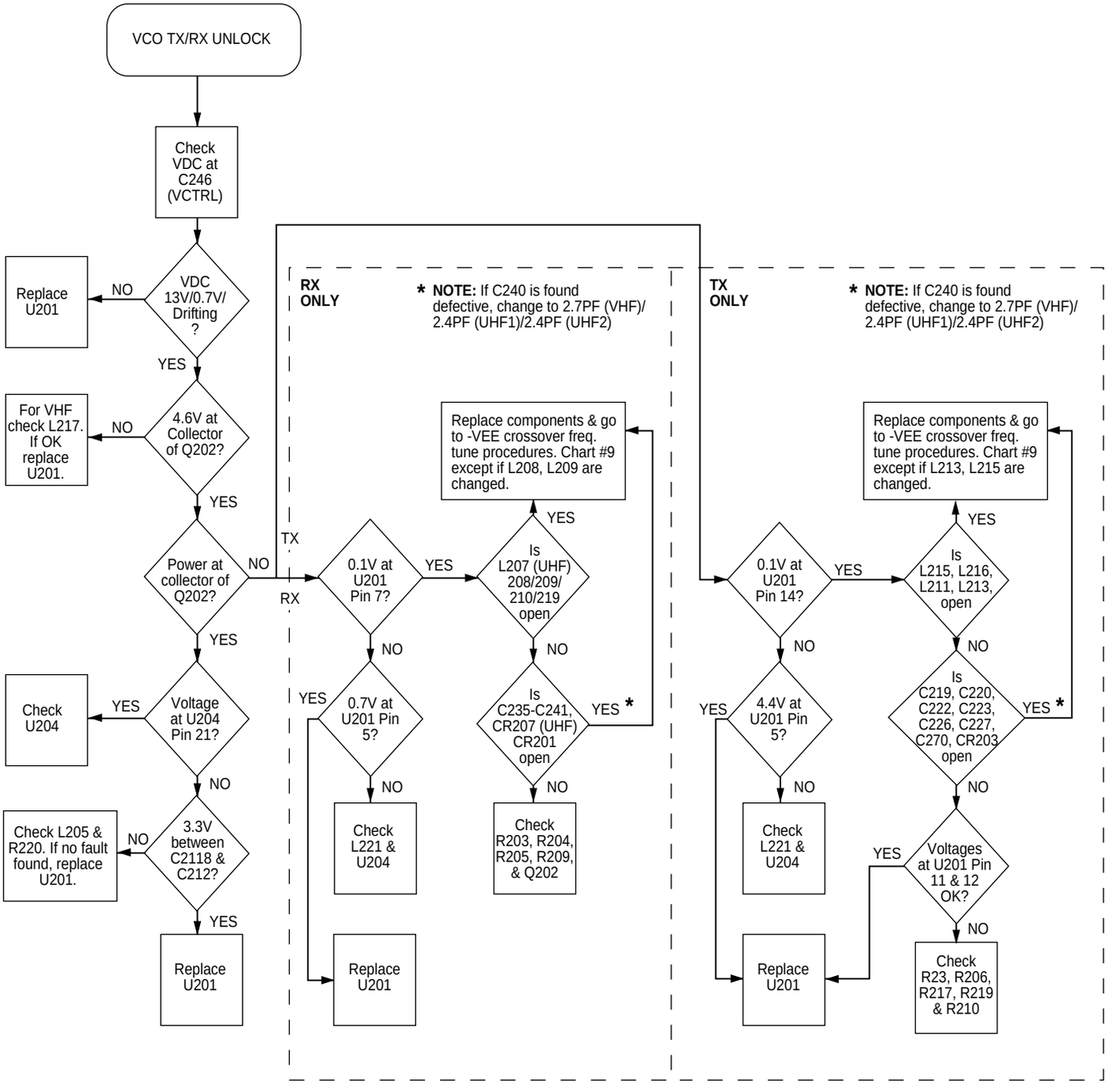


IC	PIN	VOLTAGE
U202	1, 2 8	5V 7.5V
U204	21 28 28 29 29 38 38 37 37	1.6V 1.7V (VHF TX) 1.6V (UHF TX) 1.8V (VHF RX) 1.6V (UHF RX) 4.5V (TX) 0.7V (RX) 4.5V (HIGH END) 0V (LOW END)
CR205	4	-7.5V (HIGH END) 0V (LOW END)

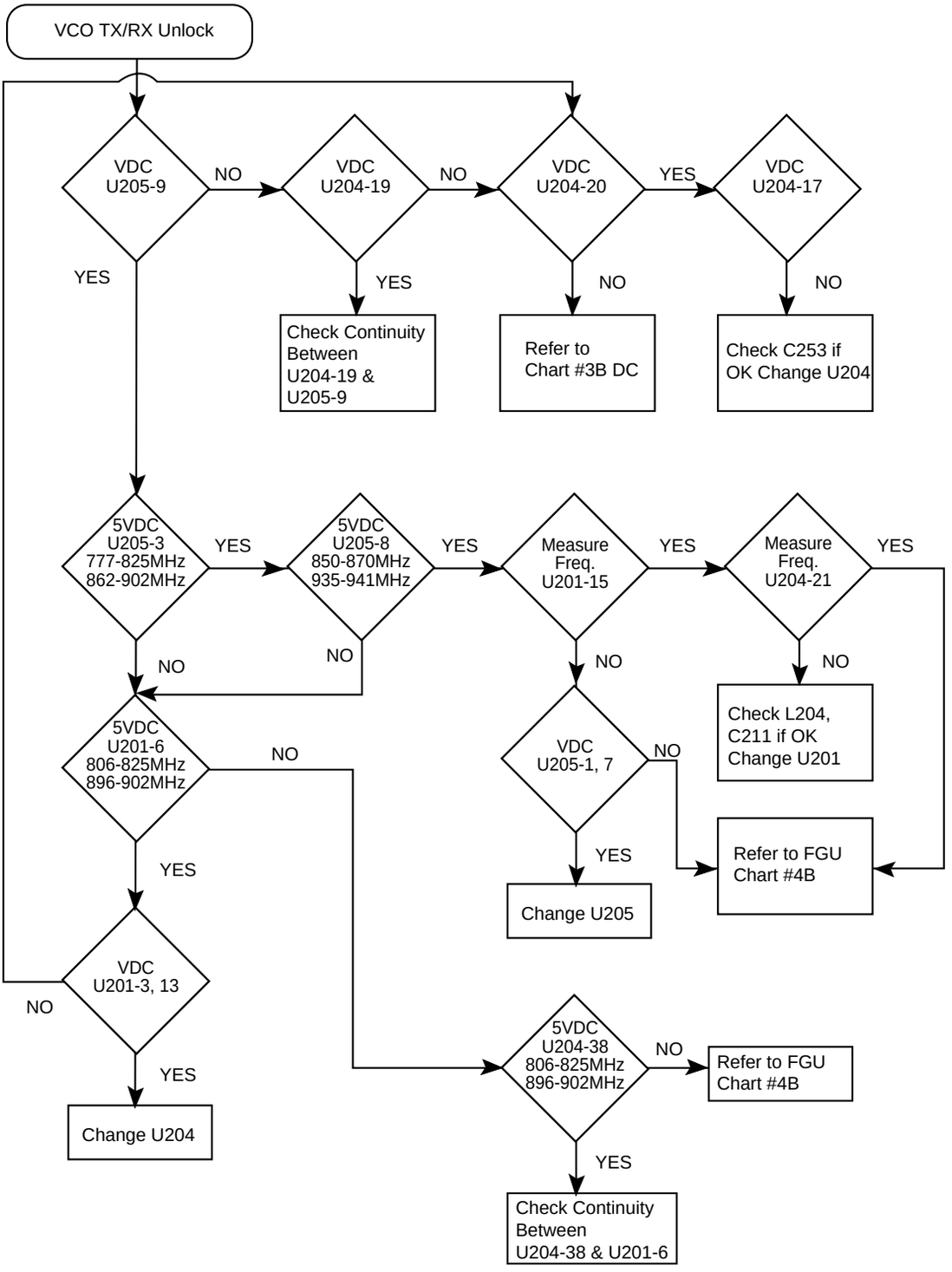
TROUBLESHOOTING FLOW CHART #4B
(800/900MHz Frequency Generation Unit - FGU)



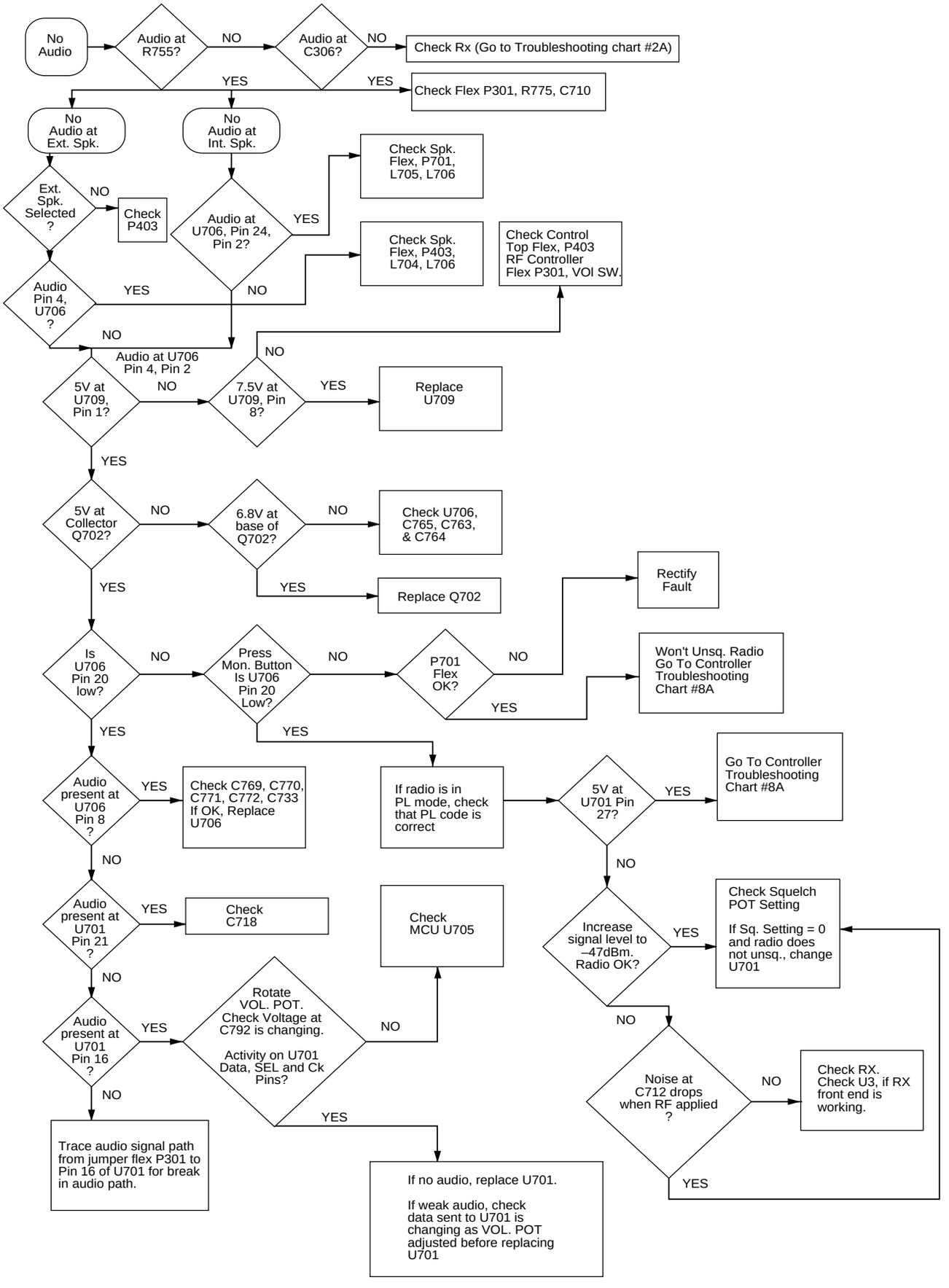
TROUBLESHOOTING FLOW CHART #5A
(VHF/UHF Voltage Controlled Oscillator - VCO)



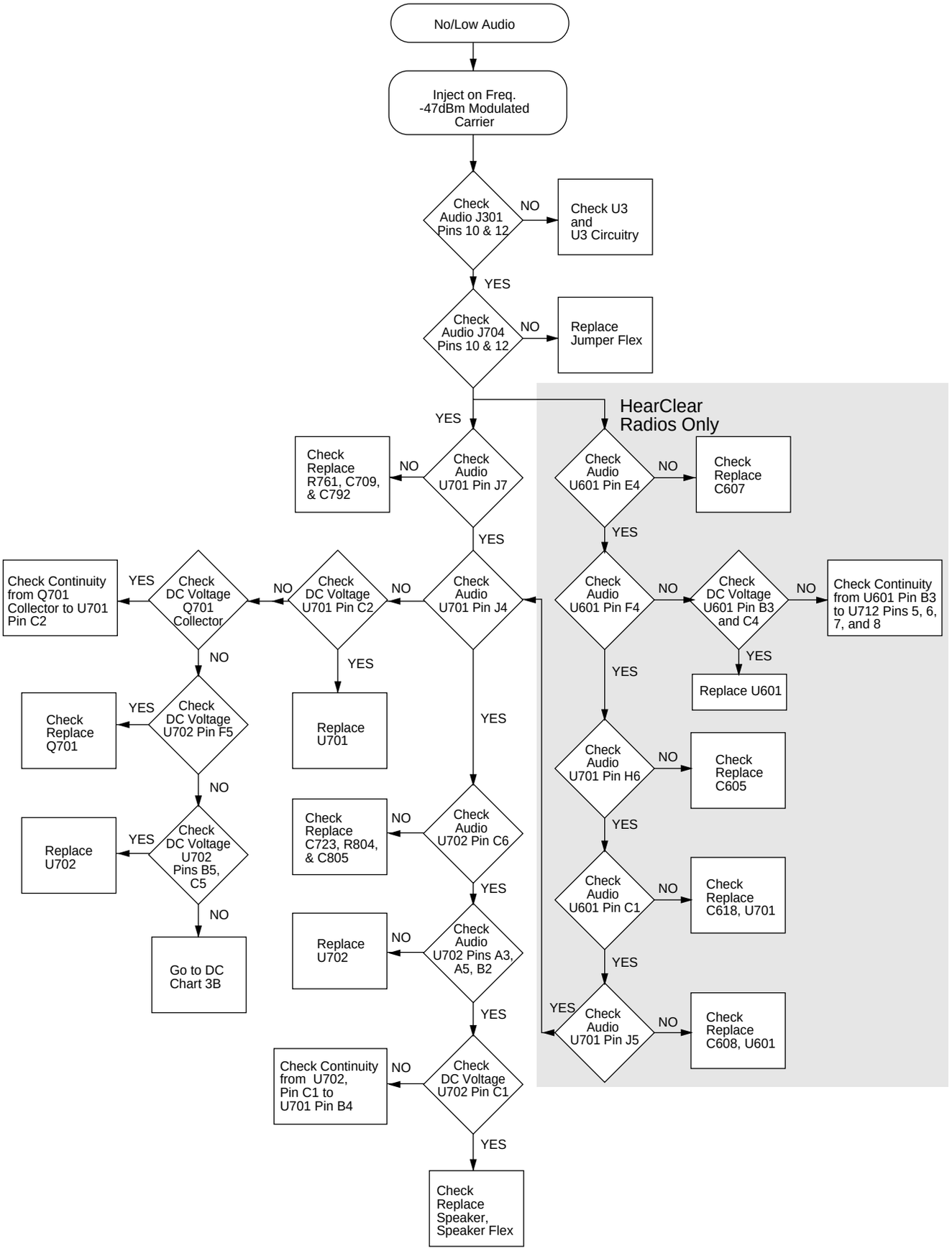
TROUBLESHOOTING FLOW CHART #5B
(800/900MHz Voltage Controlled Oscillator - VCO)



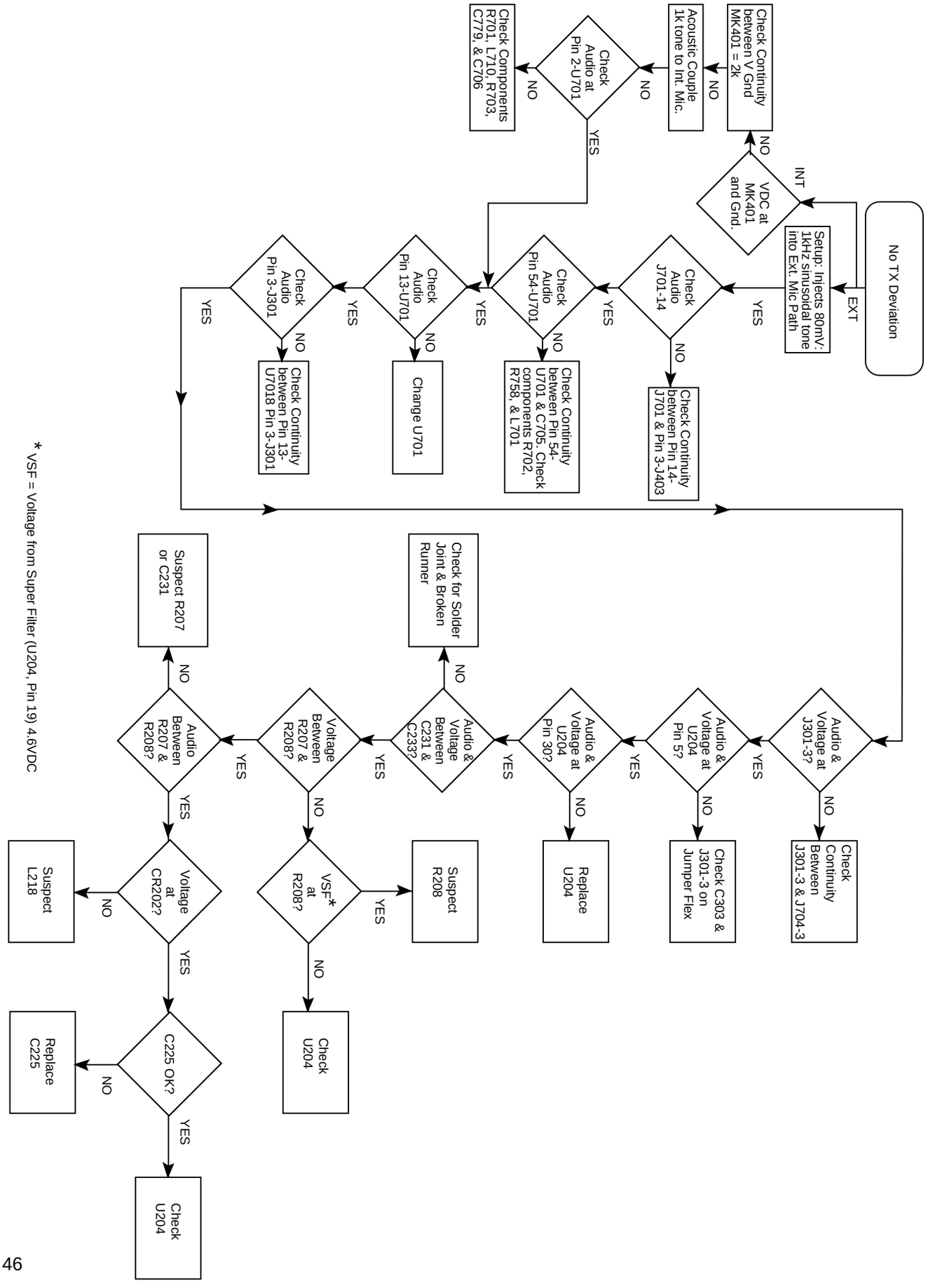
TROUBLESHOOTING FLOW CHART #6A
(VHF/UHF, Closed Architecture, No Receive Audio)



TROUBLESHOOTING FLOW CHART #6B
(800/900MHz, Open Architecture, No Receive Audio)

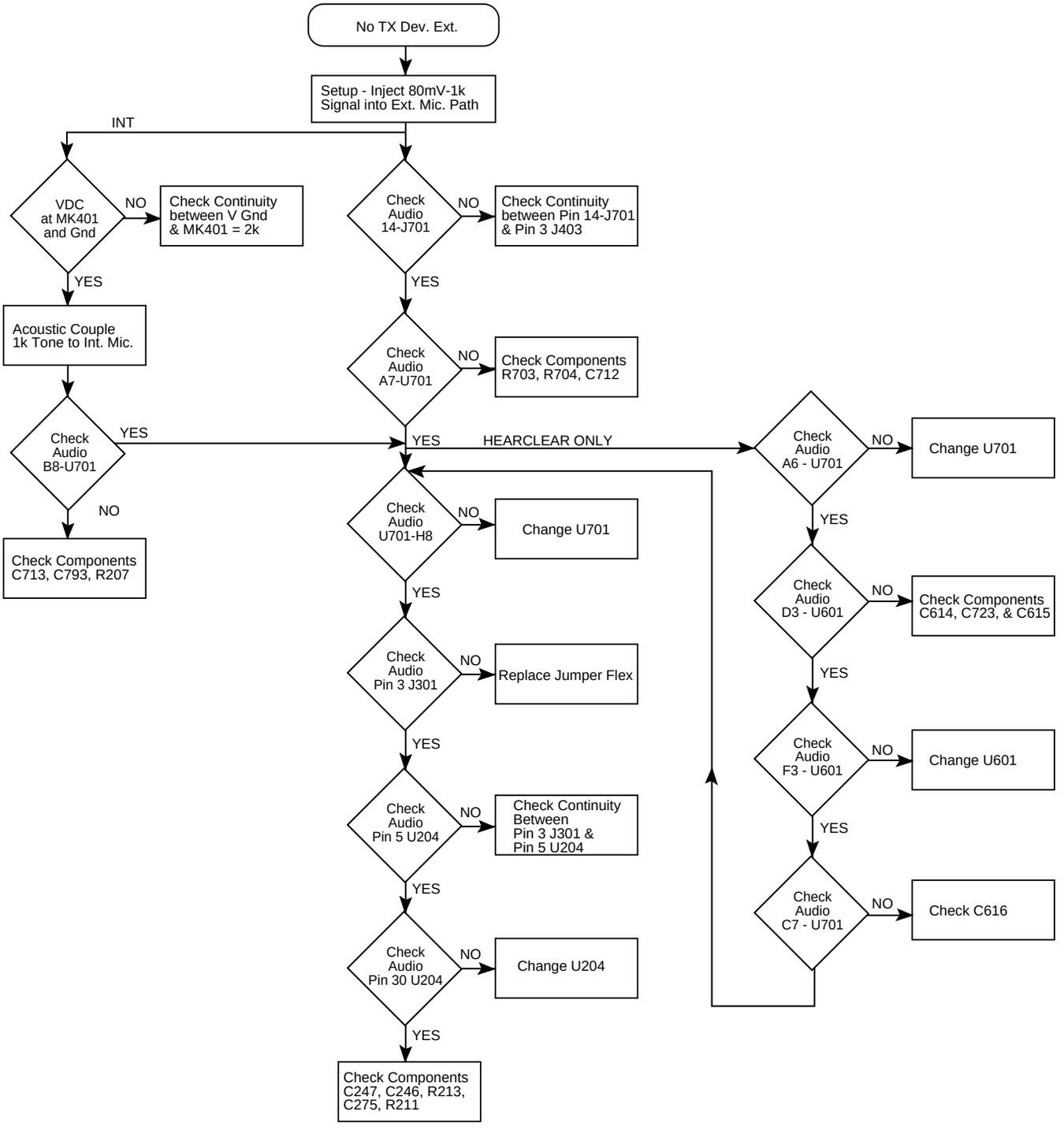


TROUBLESHOOTING FLOW CHART #7A
(VHF/UHF, Closed Architecture, No Transmit Deviation)



* VSF = Voltage from Super Filter (U204, Pin 19) 4.6VDC

TROUBLESHOOTING FLOW CHART #7B
(800/900MHz, Open Architecture, No Transmit Deviation)



TROUBLESHOOTING FLOW CHART #8A
(Closed Architecture Controller)

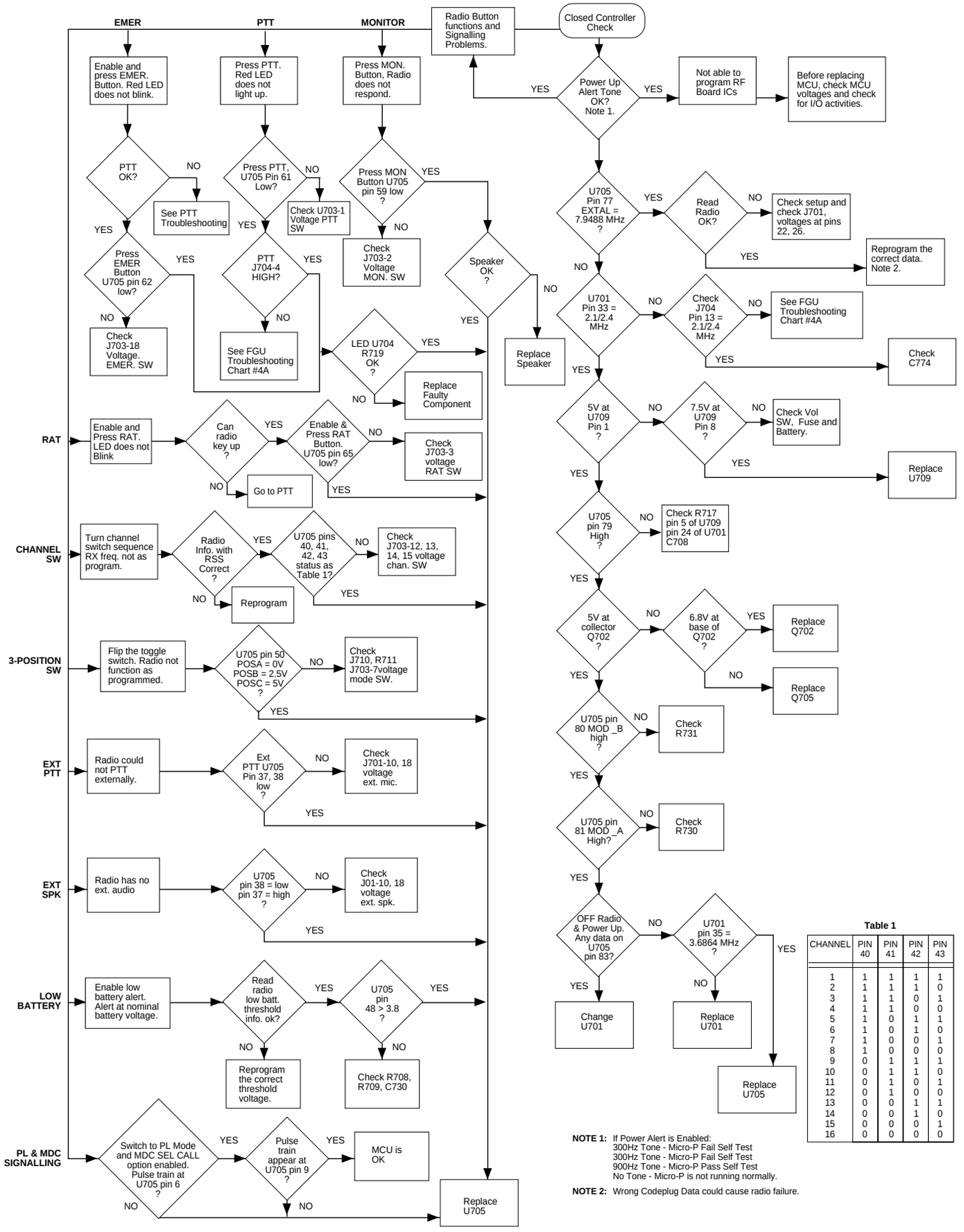


Table 1

CHANNEL	PIN 40	PIN 41	PIN 42	PIN 43
1	1	1	1	1
2	1	1	1	0
3	1	1	0	1
4	1	1	0	0
5	1	0	1	1
6	1	0	1	0
7	1	0	0	1
8	1	0	0	0
9	0	1	1	1
10	0	1	1	0
11	0	1	0	1
12	0	1	0	0
13	0	0	1	1
14	0	0	1	0
15	0	0	0	1
16	0	0	0	0

NOTE 1: If Power Alert is Enabled:
300Hz Tone - Micro-P Fail Self Test
300Hz Tone - Micro-P Fail Self Test
900Hz Tone - Micro-P Pass Self Test
No Tone - Micro-P is not running normally.

NOTE 2: Wrong Codeplug Data could cause radio failure.

TROUBLESHOOTING FLOW CHART #8B
(Open Architecture Controller)

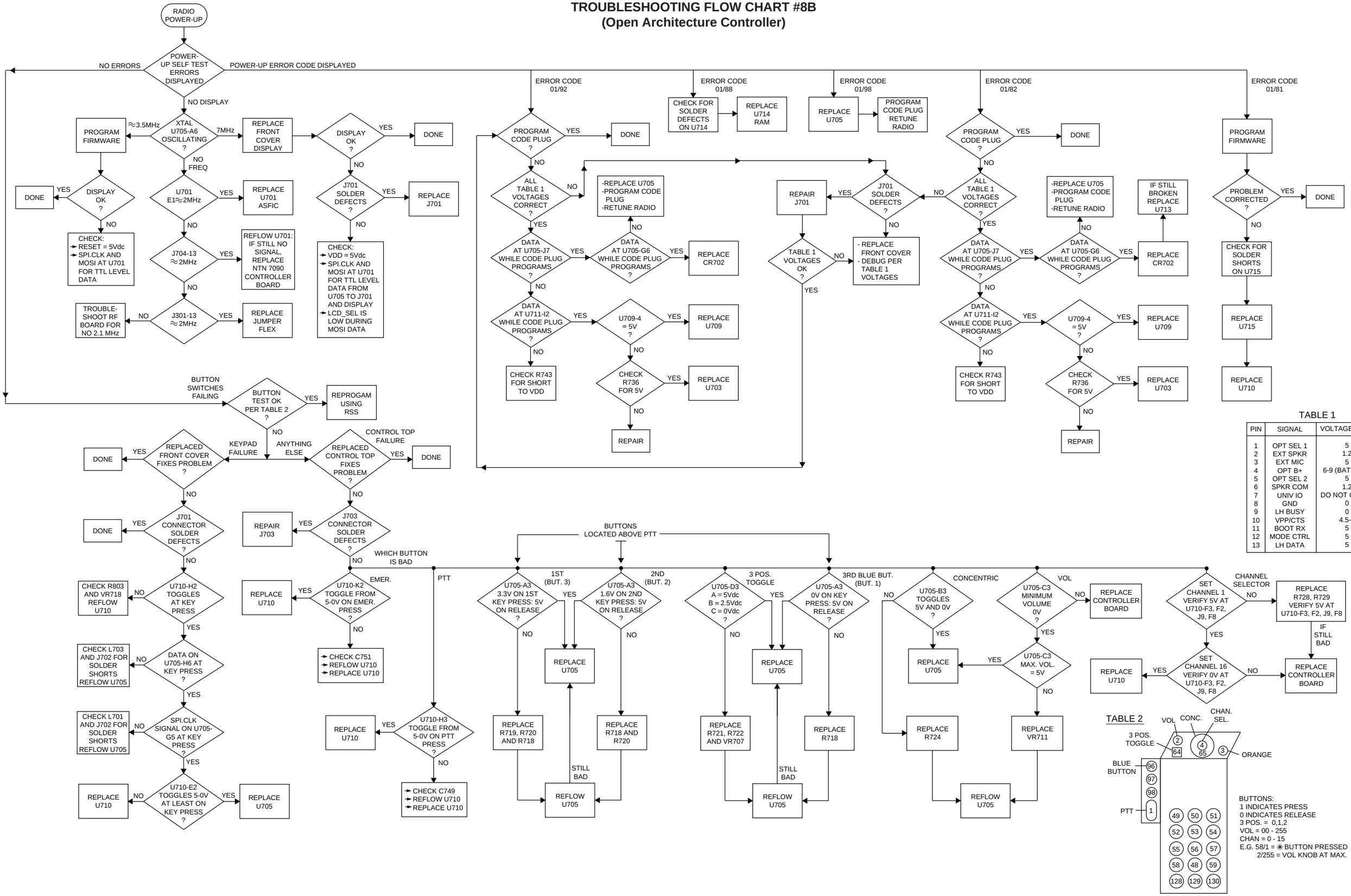


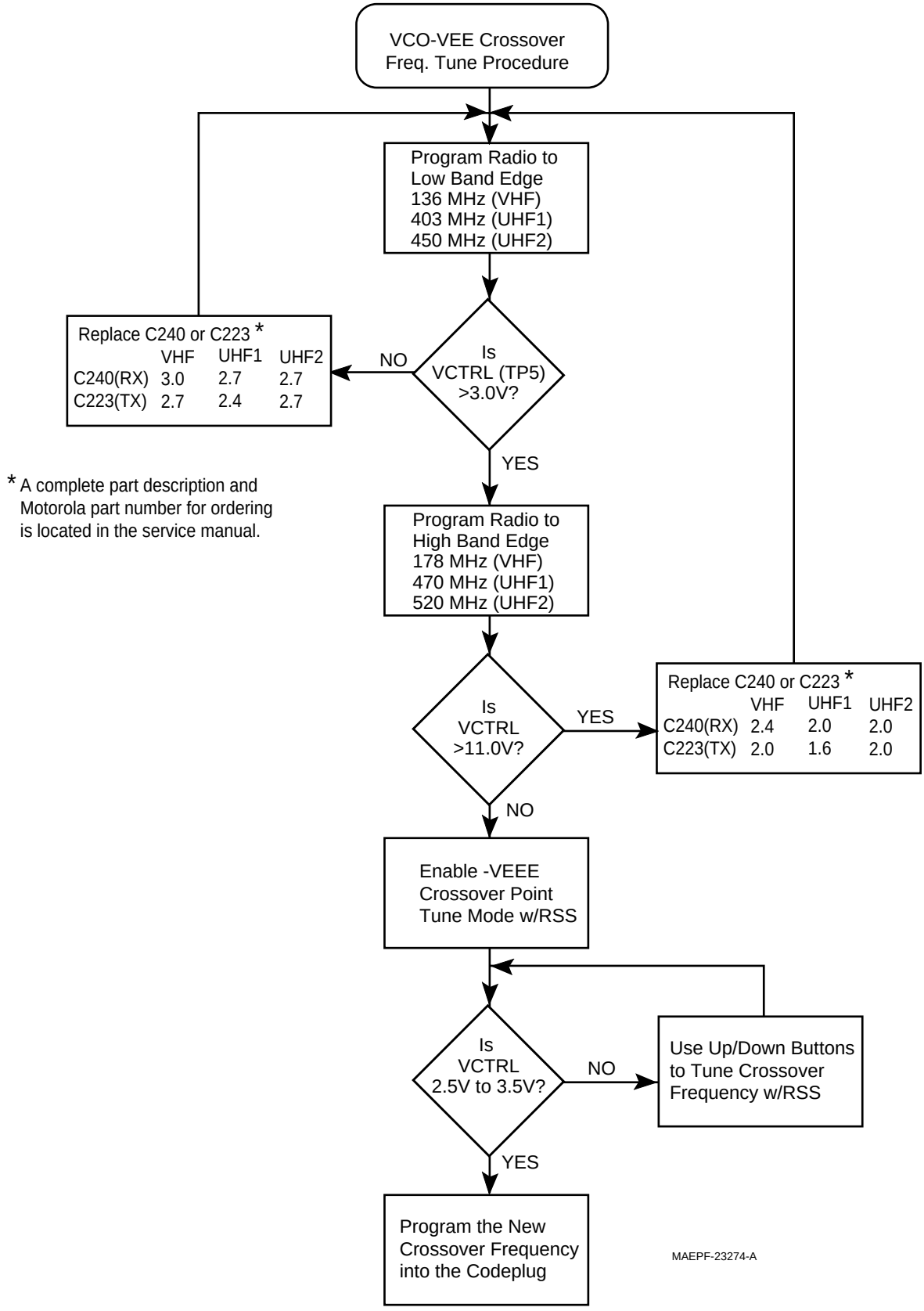
TABLE 1

PIN	SIGNAL	VOLTAGE (VDC)
1	OPT SEL 1	5
2	EXT SPKR	1.2
3	EXT MIC	5
4	OPT B+	6-9 (BATTERY)
5	OPT SEL 2	5
6	SPKR COM	1.2
7	UNIV IO	DO NOT CHECK
8	GND	0
9	LH BUSY	0
10	VPP/CTS	4.5-5
11	BOOT RX	5
12	MODE CTRL	5
13	LH DATA	5

TABLE 2

BUTTONS:
1 INDICATES PRESS
0 INDICATES RELEASE
3 POS. = 0,1,2
VOL = 00 - 255
CHAN = 0 - 15
E.G. 58/1 = ✳ BUTTON PRESSED
2/255 = VOL KNOB AT MAX.

TROUBLESHOOTING FLOW CHART #9
(VHF/UHF Only, VCO Crossover Frequency Tune)



* A complete part description and Motorola part number for ordering is located in the service manual.

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